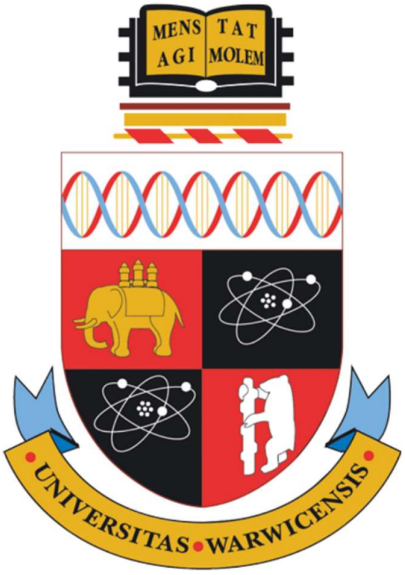
Reliability of Wide Bandgap Semiconductor Devices Under Unconventional Mode Conduction



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DECLARATION

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has not been submitted for a degree at any other University. Except where specifically stated, all of the work described in this thesis was carried out by the author or under his direction in the School of Engineering at the University of Warwick from October 2012 until July 2017

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I would like to thank my wife that joined me in this journey at its latest leg. She had to endure probably the worst of it because I had to write my thesis while working at the same time. She was there for me no matter what.

Finally, I would like to thank my family. My father and my mother with whom I would not to be the man I am today. They never gave up on me and where supporting every step of the way. My sister that was never shy on telling me how proud she is for me. Thank you all

Abstract

The use of power electronics is increasing in an exponential form. The need of power devices to be faster, block higher voltages and reduce their losses is leading to a fundamental change in the device architecture and choice of material. Gallium nitride and Silicon carbide are the materials of choice and commercial devices are available. Diamond and gallium oxide are materials that are considered for the future and they will push the boundaries of power electronics even further. There are well developed tools that can simulate the behavior of a power device is a very accurate way and they can calculate losses, turn on and turn off times and the over behavior of the device during switching. These tools are usually very complex and difficult to learn. They also cannot provide very quick results and they heavily depend on the amount of computational power that is available to the user. Due to their complexity they can only calculate a few maybe a couple of switching events before they run out of computational memory. This thesis is trying to solve this problem by using simple state space analysis and using a lot simpler equations and computational methods to predict the behavior of the device. The simplicity of these calculations can give faster results that is very helpful in a lot of cases. Also tools that calculate the temperature of the power devices have been created again using simpler mathematical equations that can evaluate the device temperature. So a fast, reliable and simple way of estimating the device behavior has been created.

Another aspect that has been covered in this thesis is the reliability of power devices under unconventional conduction. A number of devices have been tested under avalanche mode conduction and an extensive comparison has been made between device architecture, MOSFET vs IGBT, Si vs SiC, Repetitive vs single avalanche events. Also these tests have been conducted in different ambient temperatures so the effect of temperature has been investigated thoroughly as well.

1. Introduction

1.1. Power Electronics for the Power System

Global energy consumption has been increasing since the industrial revolution and there is no expectation that this is to decrease in the future. The dual concerns of energy security and the need to de-carbonize energy production has re-focused industrial and academic research on improving the efficiency of energy generation, transmission distribution and consumption. The increased electrification of heat and transportation is seen as a means of achieving these dual objectives, however, this is placing significant stress on the electrical power system. Electrification of heat and transportation in a power system with increased renewable energy injection is increasingly seen as a desirable method for de-carbonizing industrial economies as well as ensuring energy security. However, this is placing increasing stress on the electrical power network. Renewable sources of electrical power like wind and solar sources require seamless interconnection with the AC power system using power electronic converters and devices. The goal of this research proposed in this thesis is to investigate the reliability of one of the most important and fundamental components in these power converters, namely the power semiconductor device known as the SiC power MOSFET. Subsequent sections of this introductory chapter and the thesis will present the theories and methodologies employed in this research.

The traditional electrical power system is comprised of an interconnection of rotating synchronous generators, 3 phase AC power transformers, high voltage overhead transmission lines, medium/low voltage distribution cables and other ancillary components like circuit breakers, fault current limiters etc. The source of mechanical power for the electrical generators has traditionally been potential energy from moving water (for hydroelectric facilities) and reciprocating fossil fuel powered engines coal, diesel and gas fired power stations. The power

system for the overwhelming majority of its history has been based on AC transmission as a result of Tesla's development of the power transformer. However, with the development of off-shore windfarms and solar farms has made high voltage direct current (HVDC) an increasingly popular and unavoidable means of transmitting power. Furthermore, the need to connect asynchronous power systems for the purpose of facilitating bulk power transfer is also increasingly gaining popularity. The 2 GW HVDC link between France and the UK and HVDC connections between the UK and Ireland are prime examples of how HVDC connection between asynchronous power systems is gaining traction. Even power systems operating at different frequencies can be connected together using HVDC links for example in Japan and South America where 50 Hz and 60 Hz power systems exist in close proximity. HVDC has also been used for the purpose of bulk power transmission over long distances in vast countries like Canada and China where hydroelectric facilities are located very significant (thousands of kilometers) away from industrial/domestic load centers.

Traditional HVDC converters have been implemented as line commutated current source converters. In these converters, the DC current is constant and the polarity of the DC side voltage determines the direction of power flow. Since the DC side voltage can have both negative and positive polarity, then the power semiconductor devices should be capable of blocking voltages in both directions i.e. capable of exhibiting forward and reverse blocking capability. Such a device is a thyristor which is a 4 layer semiconductor device comprising of PNPN layers. Figure 1.1-1 shows a simplified thyristor schematic and circuit symbol as well as a packaged thyristor wafer and a stack of series connected thyristors for high voltage applications. The bi-directional voltage blocking capability of thyristors arises from the fact that there are 3 internal PN junctions, J1, J2 and J3 as can be seen from Figure 1.1-1. Hence, when the device is in forward blocking mode with a positive voltage on the anode with respect to the cathode, junction J1 and J3 are forward biased and junction J2 is reverse biased[1]. The

voltage blocking capability of the thyristor under forward blocking mode depends on the breakdown voltage of the junction J2.

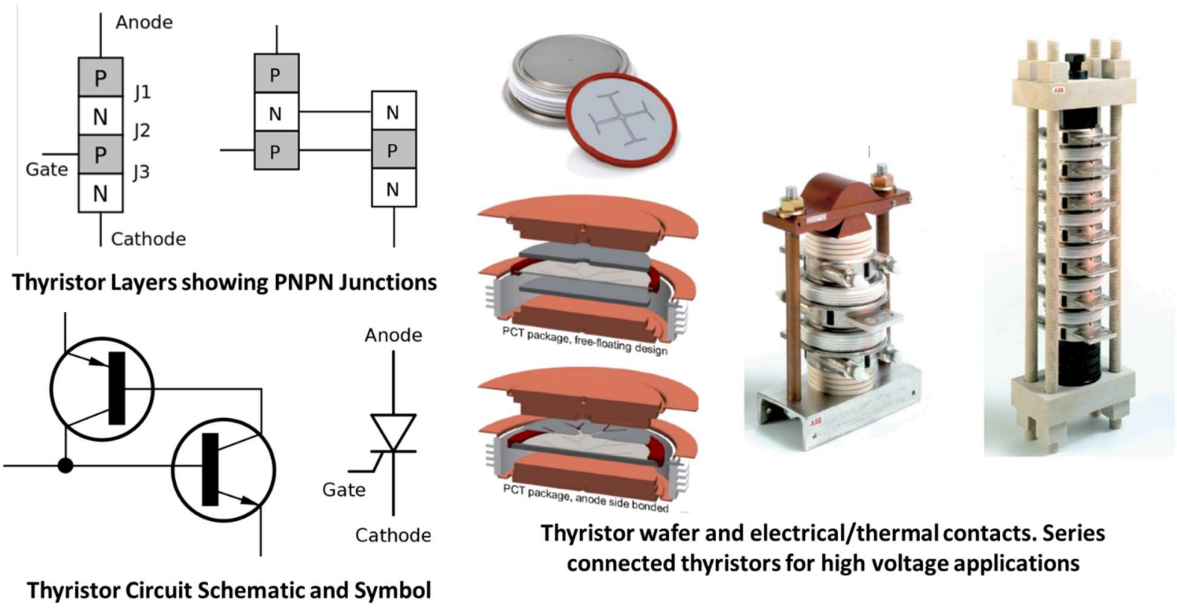


Figure 1.1-1 Thyristor schematic diagrams, packaged thyristors and series connected thyristors for high voltage applications [2]

If the forward voltage is increased beyond the rated breakdown voltage of junction J2, then the device conducts in avalanche mode. The injection of current through the gate if the thyristor reduces the breakdown voltage of junction J2, hence, the firing of the gate triggers forward mode conduction. The phase angle of the AC cycle at which the thyristor gate is fired will determine the polarity of the DC side voltage of the current source converter. If a negative anode-to-cathode voltage is connected across the thyristor, then junctions J1 and J3 are reverse biased while junction J2 is forward biased. This is the reverse blocking mode of the thyristor. As can be seen in Figure 1.1-1, the thyristor can also be thought of as 2 cross-coupled NPN and PNP BJT transistors with the base of BJT connected to the collector of the other BJT. In this sense, the thyristor is triggered when a positive regenerative feedback loop is closed as the increasing collector current of one BJT increases the base current of the other BJT and vice

versa. This theory is central to the latching of silicon IGBTs which will be explored further on in this thesis. Once a thyristor is latched, there are only 2 ways the device can be switched off and both depend on the external circuit, hence, thyristors do not have self-turn-off capability. To turn-off a conducting thyristor, either the current through the thyristor must fall below its holding current or the voltage across the thyristor must commutate. This is the reason why the current source converter is usually line commutated. It is based on the fact the phase-to-phase commutation of the converter is initiated by the system AC voltage since thyristor turn-off is effected that way. Figure 1.1-2 shows a 12 pulse thyristor based line commutated current source converter used in typical HVDC systems. In such converter, current commutates from one phase to another through the initiation of the system AC voltage reversal and this is based on the fact that thyristors do not have self-turn-off capability.

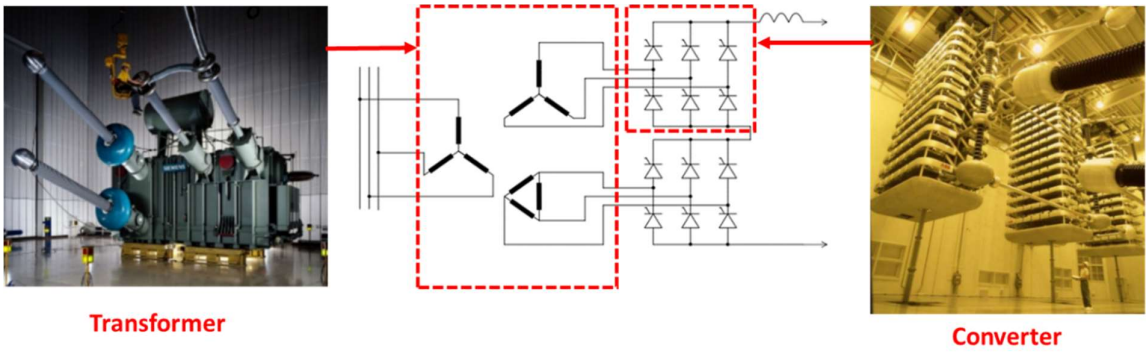


Figure 1.1-2 Typical 12-pulse line commutated current source converter [3]

In the current source converter shown in Figure 1.1-2, two 6 pulse converters are cascaded using a phase shifting transformer. The purpose of the phase shifting transformer is to shift the DC side harmonics from 6 times the fundamental frequency to 12 times its fundamental frequency. Since the current conduction mechanism of the thyristor is by avalanche mode conduction through a reverse biased PN junction, the bulk of the wafer is used to carry current as opposed to MOSFETs and IGBTs where channels adjacent to the gate are used. As a consequence, thyristors are unrivalled in their current handling capability and are thus the

devices of choice for very large GW scale power conversion. Indeed, all of the largest HVDC projects planned in the future still use line commutated current source converter technology implemented by series connected phase controlled thyristors in valve stacks. Soon after the development and deployment of these converters for point-to-point bulk power transmission over land using HVDC systems, power electronics engineers soon recognized the deficiencies of this system including (i) the need for reactive power compensation since the thyristor current always lagged the thyristor voltage (ii) the need for strong AC systems on both AC side terminals of the back-to-back system (iii) the incapability of the converter to initiate black-start i.e. synthesize 3 phase AC voltages thus acting as a virtual synchronous generator (iv) the physical size of the DC and AC side capacitors and reactors required for filtering harmonics and (v) commutation failure from thyristor misfiring. These deficiencies together with advances achieved in increasing the voltage blocking capability of fully controllable power devices like IGBTs and MOSFETs led the power electronics to the voltage source converter.

The voltage source converter is a converter that initiates power flow using the direction of the DC side current while the DC side voltage is kept constant. The power devices are fully controllable in the sense that it possesses self-turn-off capability, hence, the flow of current can be interrupted. Because the direction of power flow is determined by the direction of the DC side current, each power device possesses bi-directional current flow capability. This is achieved using a transistor with a diode connected in anti-parallel. Unlike the line commutated current source converter where phase-to-phase current commutation is initiated by the AC power system at the system frequency (50 Hz or 60 Hz), in self-commutated voltage source converters, phase-to-phase current commutation is initiated by the gate drivers of the power transistors enabling turn-on and turn-off. This is a benefit of having fully controllable devices. Hence, as a result, the switching frequency of the converter can be increased thereby shifting the harmonics to higher frequencies that can easily be filtered using small and compact

capacitors and reactors. Hence, VSC-HVDC systems are significantly more compact than traditional LCC-HVDC systems. VSCs are also capable of black-starting power systems since they are fully controllable and do not rely on the AC system to initiate device switching like the classical LCC. VSCs can operate as inverters or rectifiers at leading or lagging power factor, hence, unlike CSCs are capable of 4-quadrant operation. As a result, VSCs do not require reactive power compensation like LCC systems. Figure 1.1-3 shows the circuit schematic of the 3-phase voltage source converter and an IGBT module typically used to implement such converters. When current flows through the transistor, the VSC is operating in inverter mode and when current flows through the diode, it is operating in rectifier mode.

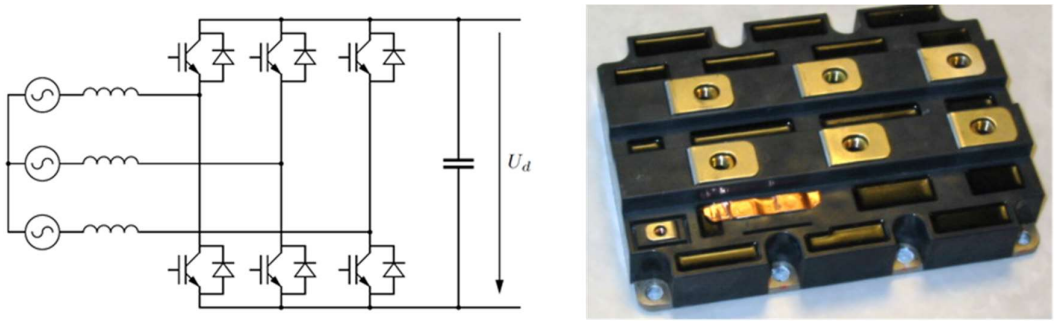


Figure 1.1-3 A Voltage source converter schematic and an IGBT power module.

The silicon IGBT is the work-horse of VSC systems in grid connected and automotive power systems. The IGBT is essentially a power device with a MOS input characteristic and a bipolar output characteristic. The IGBT has a MOS input characteristic because the gate is comprised of a polysilicon-oxide-semiconductor similar to that of a MOSFET, hence, low power voltage sourced gate driving is a significant advantage. The IGBT also has a bipolar output characteristic because it relies on conductivity modulation to achieve low conduction losses. The IGBT can be represented as shown in Figure 1.1-4, as a MOSFET with its collector connected to the base of a PNP BJT. Hence, as the MOSFET is switched on, the drain current of the MOSFET feeds into the base current of the PNP BJT. This electron current is

counteracted by a hole current that arises from hole injection from the P+ collector into the voltage blocking drift region since that PN junction is forward biased under forward blocking mode. Hence, the electrons and holes recombine in the voltage blocking drift layer thereby creating a carrier plasma that gives the device low conduction losses. However, when the IGBT is switched OFF, the need for minority carrier recombination in the voltage blocking drift region causes a long tail current in the IGBT turn-OFF characteristics. This adds to switching losses thereby making IGBTs good for delivering low conduction losses but not optimal for high frequency (several tens of KHz) applications where switching losses can be considerable. As a result, IGBTs are the power device technology of choice in medium voltage medium frequency applications while thyristors are used in high voltage low frequency applications and MOSFETs are used in low voltage high frequency applications.

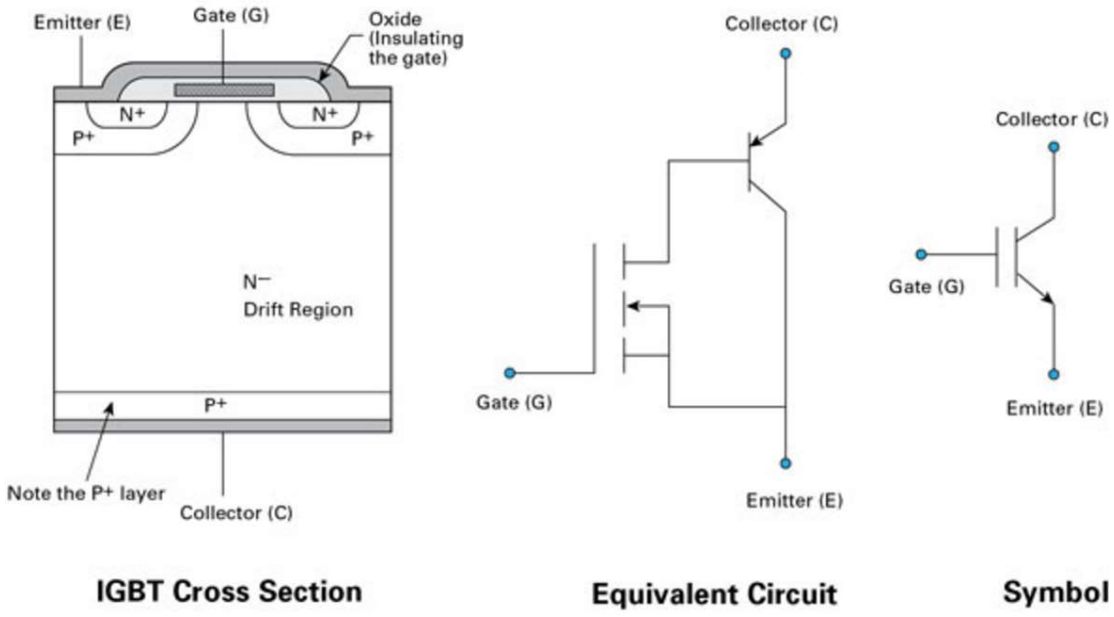


Figure 1.1-4 Schematic diagram and equivalent circuit representations

IGBTs are capable of both forward and reverse voltage blocking since the forward voltage is blocked by the p-body to drift PN junction and the reverse voltage is blocked by the p-collector to N-drift PN junction. The IGBT schematic shown in Figure 1.1-4 is a symmetric IGBT or a

non-punch-through (NPT) IGBT. It is a symmetric IGBT because its forward and reverse blocking voltages will theoretically be equal. It is also referred to as an NPT IGBT because under its maximum forward blocking capability, the depletion region formed by the reverse biased p-body to N drift junction does not extend to the p+ collector. Hence, the thickness of the drift layer must be sufficient to block the full voltage rating of the device. In a punch-through IGBT, an N+ buffer layer is inserted between the p+ collector and the N- voltage blocking drift layer. The purpose of this N+ buffer layer is to act as a field stopper. Punch-through IGBTs are also known as Field-Stop IGBTs or Asymmetric IGBTs. IGBTs can come in discrete packages like the TO-247 or power modules with DBC substrates as shown in Figure 1.3. As stated previously, IGBTs are limited in switching frequency because of the tail current resulting from carrier recombination during turn-OFF. In low voltage applications (sub 500 V) where high switching frequencies are used, like switch mode power supplies, MOSFETs are the technology of choice.

Power MOSFETs are unipolar devices that rely solely on the drift of majority carriers as opposed to IGBTs which are bipolar devices that rely on the diffusion of minority carriers. The voltage blocking capability of a power MOSFET is determined by the thickness and doping of the voltage blocking drift layer. Since the conduction losses increase with the voltage rating, power MOSFETs are limited in the voltages they are capable of blocking since conduction losses become unacceptable. IXYS has commercialized a 1.2 kV power MOSFET, however, the conduction losses are unacceptably high [4]. As a result of its unipolar characteristics, MOSFETs switch very quickly since the inter-terminal parasitic capacitances and gate resistance are the only limiting factors. Improving the conduction losses of power MOSFETs will require either increasing the active area or using trench or U-MOSFET architectures. However, both have the consequence of increasing the parasitic capacitances thereby increasing the switching losses. Hence, there is a trade-off between conduction and

switching losses in the design of power MOSFETs. One method of significantly improving the conduction losses of power MOSFETs without increasing the switching losses is to use an alternate semiconductor material with a high critical electric field. The critical field of a power semiconductor is the maximum internal electric field the material can sustain before breaking down in avalanche mode conduction via impact ionization. Using a material with a high critical electric field means that the voltage blocking drift layer can be thinner and more highly doped without losing any of its voltage blocking capability. Materials with wide energy bandgaps tend to have high critical electric fields since more thermal energy is required for generating electron-hole pairs. One such material is silicon carbide, a well-known wide bandgap semiconductor. By using SiC, power MOSFET technology can be pushed into IGBT voltage blocking domains while maintaining the low loss and fast switching capability of the MOSFET. Hence, SiC power MOSFETs and Schottky diodes have begun a revolution in power electronics. Much of the focus of this thesis is on SiC power MOSFETs.

1.2. The Power MOSFET

The first vertical power MOSFETs were manufactured in the 1970s [5]. The motivation behind the development of the power MOSFET was to improve the performance of the existing bipolar power transistors (BJT). The problem with the BJT was the collapse in current gain in high voltage rated devices. Also the switching frequencies of BJTs are significantly lower than those of a power MOSFET as a result of minority carrier charge storage in the voltage blocking drift layer as already explained for IGBTs. Hard switching of the BJTs in high frequency applications was difficult to implement. Substituting current driven BJTs with voltage driven MOSFETs was the only solution to overcome these obstacles.

The gate impedance of a MOS transistor is theoretically infinite thereby the gate drive a lot simpler since the only current supplied is during the switching transients. Also being able

to switch the devices from 10 up to 50 kHz generated a completely new field of usage for devices like the power MOSFETs. As mentioned previously, the switching capabilities are superior to other devices however the power handling capabilities of MOSFETs remains behind that of IGBTs, BJTs and thyristors. This is due to the high impedance between the drain and the source in the forward mode since conductivity modulation is not used as in bipolar devices. The power dissipated restrains the amount of current the device can withstand as well as the efficiency. Figure 1.2-1 shows the application domains of different power device technologies and their corresponding operational frequencies and blocking voltages.

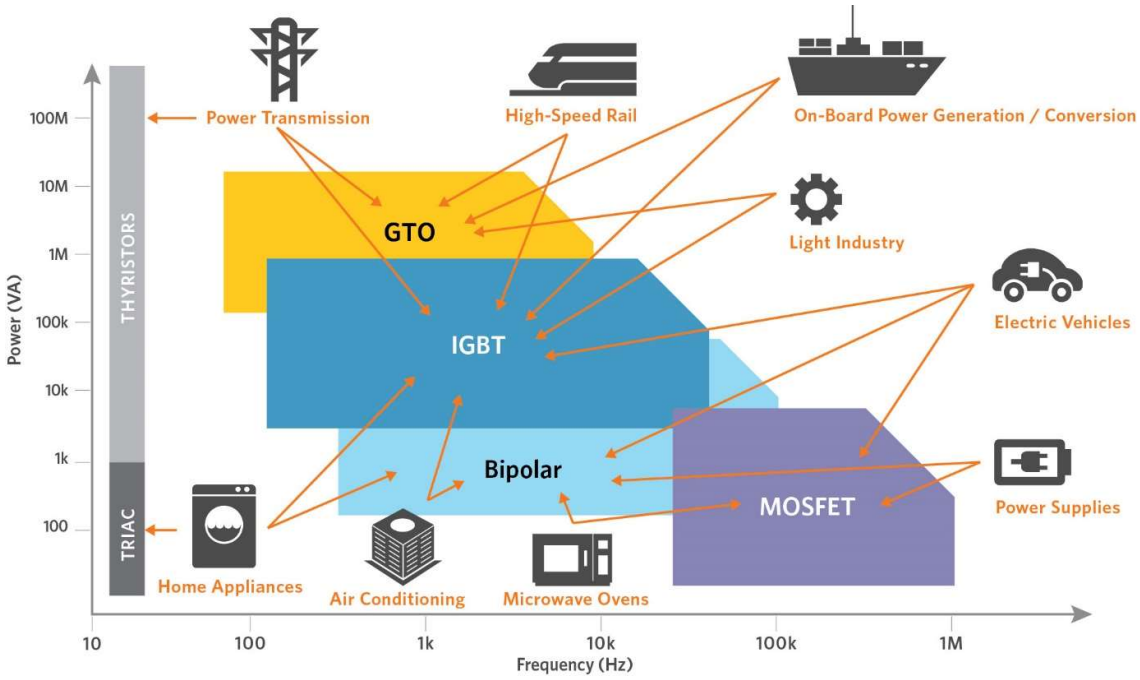


Figure 1.2-1 Application domains of different power device technologies and their corresponding voltages and Frequencies.

As can be seen from Figure 1.2-1, thyristors are used in the HVDC and other high power applications like rail traction and FACTS. IGBTs are used in rail traction, HVDC-VSC, electric vehicle and other medium voltage medium power applications. MOSFETs are used in switch mode power supplies for domestic electronic applications and other low voltage power conversion applications. The first commercial MOSFET was developed using the double

diffusion process. The channel of the device was formed by controlling the depth of two junctions. This made possible the construction of a short channel length without the need to use expensive high resolution lithography. Power MOSFETs can be lateral devices, which simply means that the path of current flow from source to drain is horizontal. These devices are called LD-MOSFETs and are still used in applications that require the integration of CMOS with power MOSFETs i.e. BCD processes or bipolar, CMOS DMOS processes. LD-MOSFETs are limited in their power handling capabilities because of the high thermal resistances since only a small portion of the semiconductor is used for current flow. In an effort to improve the power handling capability, vertical MOSFETs were developed. The primary different between a lateral and a vertical MOSFET is the fact that the drain terminal of a vertical MOSFET is at the bottom of the device, hence, the drain metallization is on the bottom of the chip while the source metallization and gate is at the top. Since the bulk of the device is used for current flow, the thermal resistance is reduced thereby increasing the power handling capability. Vertical power MOSFETs can be vertically diffused MOSFETs (VD-MOSFETs) or trench MOSFETs (also known as U-MOSFET). Figure 1.6 shows simplified cross-sections of a trench MOSFET, a VD-MOSFET and an LD-MOSFET where the doping layers can be seen. As expected, there is a trade-off between the power handing capability and the switching frequencies between the different MOSFET technologies. LD-MOS device have the high switching capability and lower handling capacity while the vertical devices can handle more power but switch less quickly.

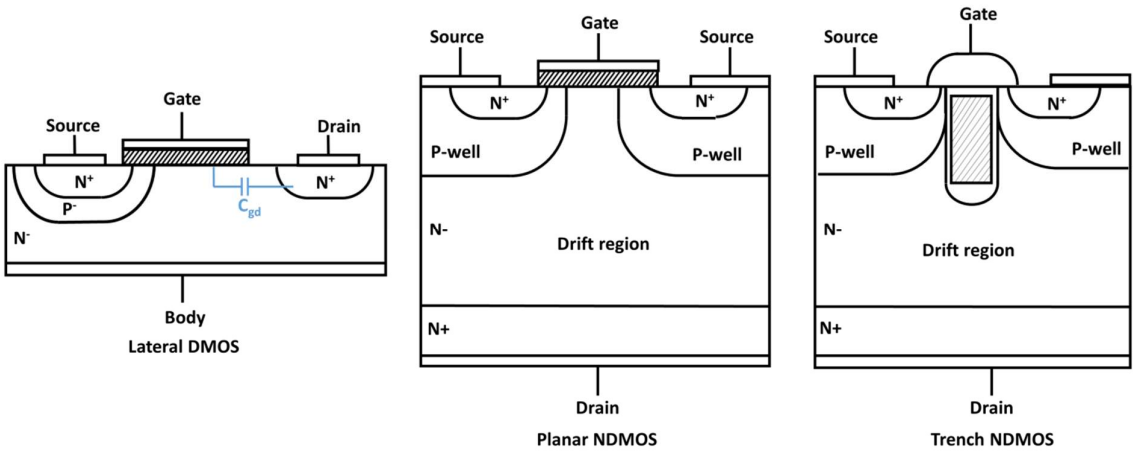


Figure 1.2-2 Planar NDMOS, Trench NDMOS and lateral DMOS Power Devices

1.2.1. Fundamentals of Power MOSFETs

Key to the understanding of the operation of the MOSFET is the operation of the MOS channel. The MOS channel comprises of a polysilicon gate, a thermally grown silicon dioxide insulator and a p-doped semiconductor through which the channel is formed. Figure 1.7 shows the band-diagram of a MOS system with the Fermi levels, electron affinities and energy bandgap of each of the layers clearly labelled. The Fermi-level is defined as the energy level within the semiconductor in which there is a 50% chance of electron occupation. The Fermi level depends on the doping of the layer and varies between the conduction band and valence band. The electron affinity is the energy difference between the conduction band of the material and the Vacuum level while the energy bandgap is the energy difference between the conduction band and the valence band. The electron affinity of silicon is 4.05 eV while that of silicon dioxide is 0.95 eV, hence, the conduction band offset between Si and SiO_2 is 3.1 eV while the valence band offset is 4.8 eV. As a result of these high band offsets, electron and hole conduction through the gate oxide insulator is limited to very low values due to FN tunneling and direct tunneling [6]. The energy bandgap of silicon is 1.1 eV while that of SiO_2 is 9 eV. The Fermi level of the N+ polysilicon gate lies within the conduction band since it is

degenerately doped for the purpose of making its conductivity near metallic. Under equilibrium conditions, the Fermi levels in the semiconductor align.

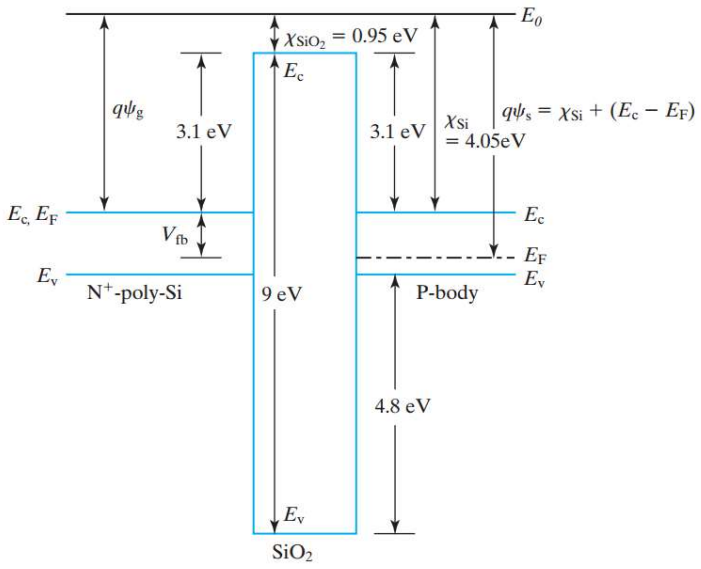


Figure 1.2-3 Energy band diagram of the MOS interface

The energy band diagram of the MOS interface shown in Figure 1.2-3 is for the flat-band condition where a negative potential has been applied at the polysilicon gate to ensure that the bands are flat at the silicon channel to gate oxide interface. The voltage required for achieving this condition is known as the flat-band voltage. This flat-band voltage is determined by the difference between the Fermi levels of the polysilicon gate and the silicon channel. Since for an n-type MOSFET, the polysilicon is degenerately doped n-type while the body is doped p-type, then the flat-band voltage is non-zero. The energy difference between the Fermi level and the Vacuum level is known as the work-function of the material. Because the Fermi level depends on the doping of the semiconductor layer, then the work-function also depends on the doping. The flat-band voltage can be expressed in equation (1.2-1) as a difference between the metal/semiconductor work-function difference and the fixed oxide charge in the gate oxide insulator.

$$V_{fb} = (\varphi_m - \varphi_s) - \frac{Q_F}{C_{OX}} \qquad (1.2\text{-}1)$$

As the gate voltage on the MOS channel is increased from negative to positive, the MOS device goes through 3 stages namely, accumulation, depletion and inversion. Figure 1.8 shows the MOS band diagram for each of these conditions.

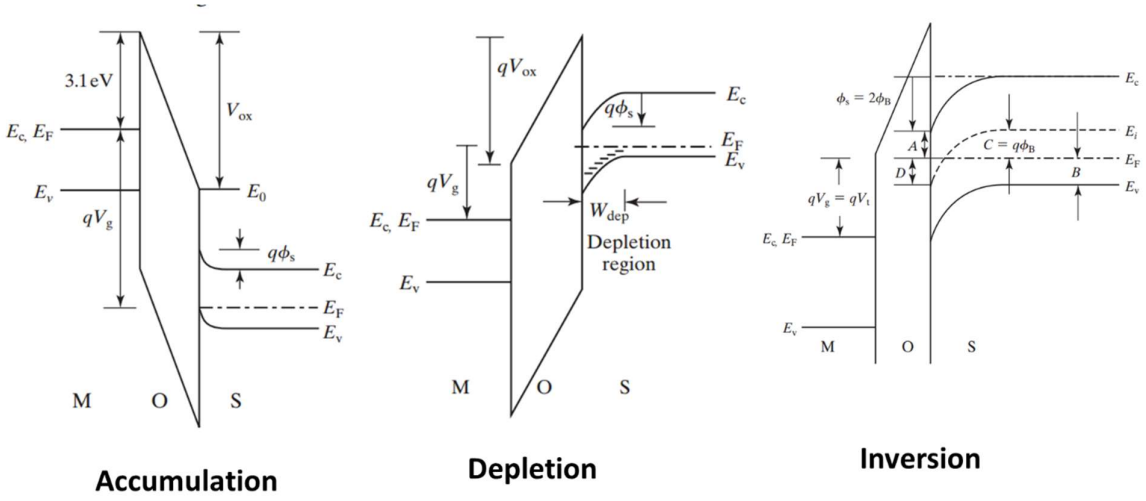


Figure 1.2-4 MOS band diagram for accumulation, depletion and inversion

When a negative voltage is applied on the MOS gate, the gate bands are pushed upwards in proportion to the magnitude of the negative voltage. The valence band of the p-substrate bends upwards towards the Fermi level of the p-substrate by an amount that is equal to the surface potential (Φ_S). The total gate voltage is the sum of the surface potential voltage, the flat-band voltage and the voltage supported by the oxide according to equation (1.2-2)

$$V_g = V_{fb} + \phi_s + V_{OX} = \left((\varphi_m - \varphi_s) - \frac{Q_F}{C_{OX}} \right) + \phi_s + V_{OX} \qquad (1.2\text{-}2)$$

Since the valence band of the p-substrate bends towards the Fermi level, the surface concentration of the holes exceeds the doping concentration of the p-substrate according to equation (1.2-3)

$$p_s = N_A e^{\frac{q\phi_S}{K_B T}} \qquad (1.2\text{-}3)$$

Because, there is an accumulation of majority carriers in the channel, this condition of the MOS system is known as "*accumulation*". According to Gauss's law, the total accumulation charge (Q_{ACC}) and voltage across the oxide (V_{OX}) can be calculated as

$$E_{OX} = \frac{V_{OX}}{t_{OX}} = -\frac{Q_{ACC}}{\varepsilon_{OX}} \qquad (1.2\text{-}4)$$

By combining equations (1.2-4) and (1.2-2) the accumulation charge can be expressed as

$$Q_{ACC} = -\varepsilon_{OX} E_{OX} = -\frac{\varepsilon_{OX}}{t_{OX}} V_{OX} = -C_{OX}(V_g - V_{fb} - \phi_s) \qquad (1.2\text{-}5)$$

As the gate voltage becomes less negative and exceeds the flat-band voltage, the p-substrate bands first flatten and then bend downwards in the opposite direction. Since the conduction band bends towards the Fermi-level and the valence band bends away from the Fermi level, the majority carrier concentration reduces or "*depletes*". This is known as depletion. It can be seen from equation (1.2-3) that the hole carrier concentration will reduce as the surface potential (Φ_S) becomes positive. From Gauss's law, the depletion charge and the surface potential can be expressed as equations (1.2-6) and (1.2-7) respectively.

$$Q_{dep} = \varepsilon_{Si} E_{Si} = qN_A W_{dep} = C_{OX} V_{OX} \qquad (1.2\text{-}6)$$

$$\phi_S = \int_0^{W_{dep}} E_{Si} dx = \int_0^{W_{dep}} \frac{qN_A x}{\varepsilon_{Si}} dx = \frac{qN_A}{\varepsilon_{Si}} \int_0^{W_{dep}} x dx = \frac{qN_A W_{dep}^2}{2\varepsilon_{Si}} \qquad (1.2\text{-}7)$$

As the gate voltage is increasingly more positive and the intrinsic Fermi level bends below the Fermi level, then the electron concentration increases and the p-type substrate becomes inverted. As shown in figure Figure 1.2-4, the p-substrate bands bend downwards and the intrinsic Fermi level and conduction bands bend towards to Fermi level while the valence band bends away from the Fermi level. The point of threshold is defined as the instant when the electron concentration in the inverted layer is equal to the hole concentration in the bulk. This occurs when the energy difference between the conduction band and the Fermi level (A in Figure 1.2-4is equal to the energy difference between the Fermi level and the valence band (B in Figure 1.2-4). In other words, E_C - E_F = E_F – E_V. The bulk potential due to the p-doping of the semiconductor can be expressed as equation (1.2-8).

$$p = N_A = n_i e^{\frac{q\phi_B}{K_B T}} \quad \Rightarrow \quad \phi_B = \frac{K_B T}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad (1.2\text{-}8)$$

Hence, since the surface potential of the semiconductor, must bend 2 times the bulk potential of the semiconductor for the point of threshold to be reached, then it follows that

$$\phi_S = 2\phi_B = \frac{2K_B T}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad (1.2\text{-}9)$$

At this point, the threshold voltage of the MOS system can be defined as the value of the gate voltage at which the electron concentration in the channel is equal to the p-type concentration in the bulk or in other words, when the surface potential is equal to twice the bulk potential. This can be expressed as equation (1.2-10).

$$V_{TH} = V_{FB} + \phi_S + \frac{\sqrt{qN_A\varepsilon_{Si}2\phi_S}}{C_{OX}} \quad (1.2\text{-}10)$$

where the surface potential is given by equation (1.2-9) and the voltage across the oxide is given by ratio of the maximum depletion charge to the oxide capacitance

$$V_{OX} = \frac{\sqrt{qN_A\varepsilon_{Si}2\phi_S}}{C_{OX}} \quad (1.2\text{-}11)$$

Equation (1.2-10) define the threshold voltage of the power MOSFET. Assuming a uniformly inverted channel between the source and the drain as shown in Figure 1.2-5, the current density of the MOSFET channel can be expressed as equation(1.2-12).

$$J = \sigma E = nq\mu_n E \quad (1.2\text{-}12)$$

Hence, the MOSFET drain current can be expressed as equation (1.2-13).

$$I = Wt_{INV}nq\mu_n E \quad (1.2\text{-}13)$$

where W is the MOSFET width and t_{INV} is the thickness of the inversion layer. The gradual channel approximation assumes that the electric field perpendicular to the gate of the MOSFET

is higher than that parallel to the gate of the MOSFET while the charge sheet approximation assumes that the MOSFET channel can be approximated as a thin sheet of charge adjacent to the gate. Using the charge sheet approximation and the gradual channel approximation [6], equation (1.2-13) can be re-written as equation (1.2-14) as shown below.

$$I = WC_{OX}\mu_n(V_{GS} - V_{TH} - V_X)\frac{dV_X}{dy} \tag{1.2-14}$$

Integrating equation (1.2-14) over the channel length of the MOSFET will yield the final expression of the MOSFET drain current as shown in equation (1.2-15).

$$\int_0^L I dy = W\mu_n C_{OX}\int_0^{V_{DS}}(V_{GS} - V_{TH} - V_X)dV_X$$

$$I_{DS} = \frac{W\mu_n C_{OX}}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{1.2-15}$$

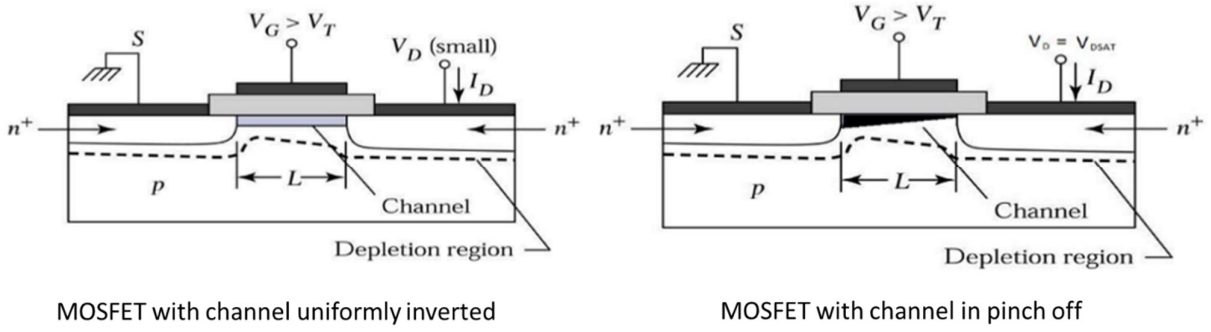


Figure 1.2-5 MOSFET with uniformly inverted channel and channel in pinch-off

Equation (1.2-15) shows that as long as the channel is uniformly inverted, the drain current will increase monotonically with the drain voltage. However, as the drain voltage of the MOSFET is increased, the drain depletion formed by the reverse biased drain to body junction causes the channel to pinch off as shown in Figure 1.2-5 MOSFET with uniformly inverted

channel and channel in pinch-off. At this point, the drain current no longer increases monotonically with the drain voltage and the MOSFET goes into saturation. Figure 1.2-6 MOSFET output characteristics and gate transfer characteristics shows the output characteristics (drain current vs drain voltage) and the gate transfer characteristics (drain current vs. gate voltage) for a typical MOSFET.

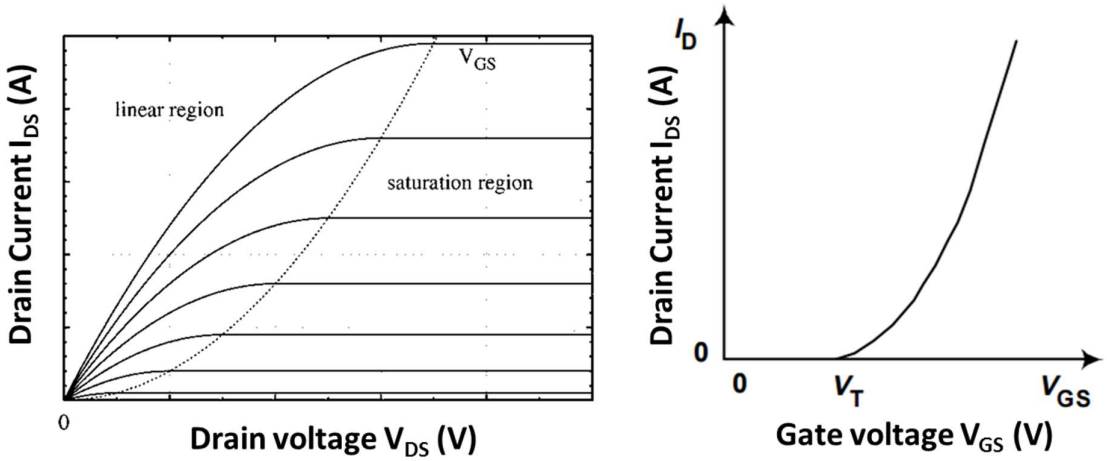


Figure 1.2-6 MOSFET output characteristics and gate transfer characteristics

If the drain-source voltage (V_{DS}) increases beyond the gate voltage overdrive ($V_{GS} - V_{TH}$), then equation (1.2-15) can be re-written as equation (1.2-16) below.

$$I_{DS} = \frac{W\mu_n C_{OX}}{2L}(V_{GS} - V_{TH})^2 \qquad (1.2\text{-}16)$$

Equation (1.2-16) is used to model a MOSFET in saturation while equation (1.2-15) models a MOSFET in the linear (triode) mode. These equations represent the steady-state models of power MOSFETs. In the next section, equations that model the switching transients of power MOSFETs are introduced.

1.2.2. Dynamic MOSFET Models

The power MOSFET is characterized by parasitic inter-terminal capacitances between the three terminals. Figure 1.11 shows the equivalent circuit of the power MOSFET with the parasitic inter-terminal capacitances along with the device cross-section showing the origin of the capacitances. The gate-source capacitance (C_{GS}) results from the overlap between the gate and the source. The oxide capacitance and overlap area contribute to this capacitance. The gate-drain capacitance is a series combination of an oxide capacitance and a depletion capacitance. This capacitance is also referred to as the Miller capacitance. Since the depletion width formed by the drain-gate junction varies with the drain voltage, then the gate-drain capacitance is non-linear over the duration of the switching transient.

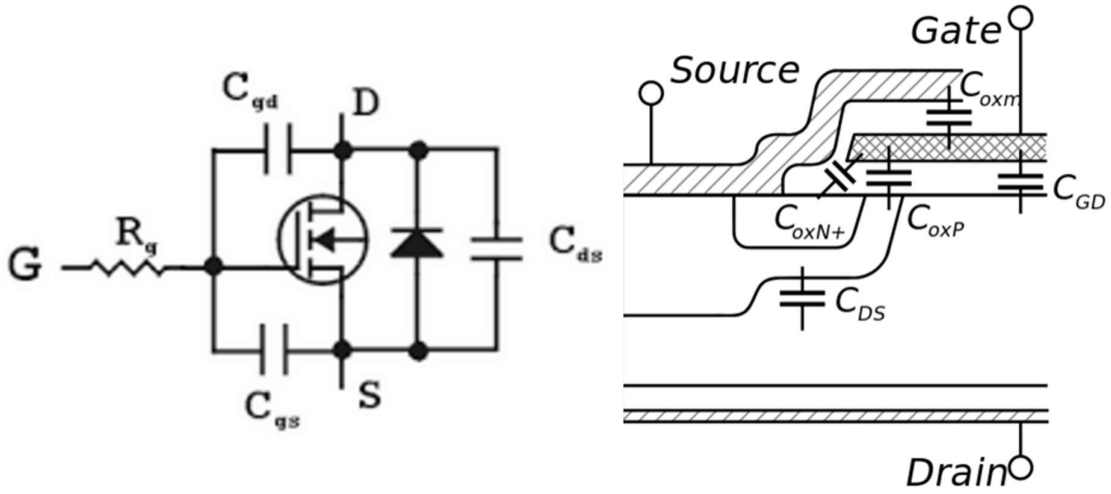


Figure 1.2-7 Equivalent circuit of power MOSFET showing parasitic capacitances.

The drain-source capacitance is also a non-linear depletion capacitance resulting from the reverse biased capacitance. The input capacitance is the sum of the gate-source and the gate-drain capacitance ($C_{GS} + C_{GD}$) while the output capacitance is the sum of the gate-drain and the drain-source capacitance ($C_{DS} + C_{GD}$).

Turn-ON Characteristics: The turn-ON characteristics of the MOSFET are analyzed in the context of switching current through an inductive load. In a VSC, current will typically commutated from a high side diode to a low side MOSFET during MOSFET turn ON and vice versa during MOSFET turn-OFF. Hence, in the analysis, it is assumed that turn-ON of the MOSFET will initiate turn-OFF of a high side diode. In the off-state, the MOSFET I_{DS} is zero, the V_{DS} is equal to the supply voltage (as the MOSFET is in forward blocking mode) and V_{GS} is zero. If the MOSFET is in a voltage source converter, then current is flowing in the other phases and depending on the phase angle on the current on the AC side, the device may or may not conduct current. When the gate driver is triggered into ON-state, the MOSFET capacitances start to charge. Figure 1.2-8 Detailed turn-ON transient *VGS*, *IDS* and *VDS* waveforms for the MOSFETshow detailed timing diagrams for the gate-source voltage (V_{GS}), the drain-source current (I_{DS}) and the drain-source voltage (V_{DS}) during turn-ON.

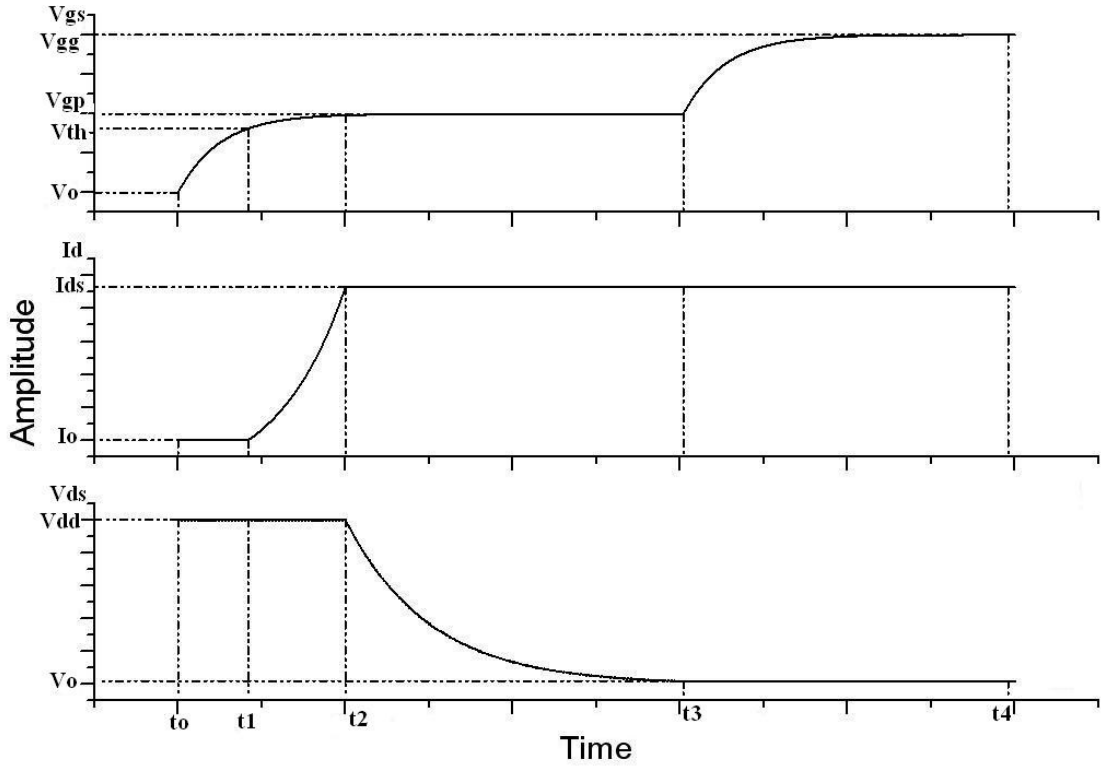


Figure 1.2-8 Detailed turn-ON transient V_{GS}, I_{DS} and V_{DS} waveforms for the MOSFET

Between time t_0 and t_1, the gate voltage rises to the threshold voltage (V_{TH}). The drain current remains at zero and the drain voltage remains at the supply voltage. During this stage, C_{GS} and C_{GD} are being charged and the equation for V_{GS} can be expressed as equation (1.2-17) below.

$$V_{GS(t)} = V_{GG}\left(1 - e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}\right) \qquad (1.2\text{-}17)$$

The time interval between the triggering of the gate pulse from the gate driver and the instant when V_{GS} becomes equal to V_{TH} is given by equation (1.2-18) below.

$$t_1 - t_0 = R_G(C_{GS} + C_{GD})\ln\left(\frac{V_{GS}}{V_{GS} - V_{TH}}\right) \qquad (1.2\text{-}18)$$

When V_{GS}=V_{TH}, the I_{DS} rises according to equation(1.2-19) below.

$$I_{DS} = \frac{W\mu_n C_{OX}}{2L}(V_{GS} - V_{TH})^2 \qquad (1.2\text{-}19)$$

The drain current increases until it reaches the load current at which point the V_{GS} becomes equal to the plateau voltage (V_{GP}). During this period, between t_1 and t_2, the Miller capacitance is charged while the V_{GS} remains constant since all of the gate current is diverted away from C_{GS} into C_{GD}. The time duration between t_2 and t_3 is given by equation below.

$$t_3 - t_2 = R_G(C_{GS} + C_{GD})\ln\left(\frac{V_{GP}}{V_{GP} - V_{TH}}\right) \qquad (1.2\text{-}20)$$

The gate voltage plateau (V_{GP}) and the gate current is calculated using equation(1.2-21) and (1.2-22) below

$$V_{GS} = \sqrt{\frac{2LI_{DS}}{W\mu_n C_{OX}}} + V_{TH} \quad (1.2\text{-}21)$$

$$I_{GP} = \frac{V_{GS} - V_{GP}}{R_G} \quad (1.2\text{-}22)$$

Between t_2 and t_3, the drain voltage falls from the supply voltage (V_{DD}) to the on-state voltage (V_{DSON}) which is given by the product of the steady-state current and the on-state resistance. The commutation rate of the drain-source voltage is given by equation (1.2-23) below.

$$\frac{dV_{DS}}{dt} = -\frac{I_{GP}}{C_{GD}} = \frac{V_{GS} - V_{GP}}{R_G C_{GD}} \quad (1.2\text{-}23)$$

Assuming a constant average Miller capacitance (C_{GDAV}), the drain voltage can be expressed as a function of time during the drain commutation transient as equation below.

$$V_{DS(t)} = V_{DD} - \frac{(V_{GS} - V_{GP})t}{R_G C_{GDAV}} \quad (1.2\text{-}24)$$

Hence, the time duration between t_2 and t_3 can also be expressed in terms of the drain voltage transient by equation (1.2-25) below.

$$t_3 - t_2 = \frac{R_G C_{GDAV}}{(V_{GS} - V_{GP})}(V_{DD} - V_{DSON}) \quad (1.2\text{-}25)$$

Between time t_3 and t_4, after the complete charging of the miller capacitance, V_{DS} is in steady state at V_{DSON} and V_{GS} resumes its exponential rise to V_{GG}. The time constant of the exponential rise is increased because of the higher value of C_{GD}.

Turn-Off Transient: In this case, it is assumed that the turn-OFF of the power MOSFET will initiate the turn-ON of the complimenting diode in the converter phase leg. Before turn-OFF commences, I_{DS} is equal to the load current, V_{DS} is equal to the produce $I_{DS} \cdot R_{DSON}$ and V_{GS} is equal to V_{GG}. Figure 1.13 shows the turn-OFF transient waveforms for V_{GS}, I_{DS} and V_{DS}.

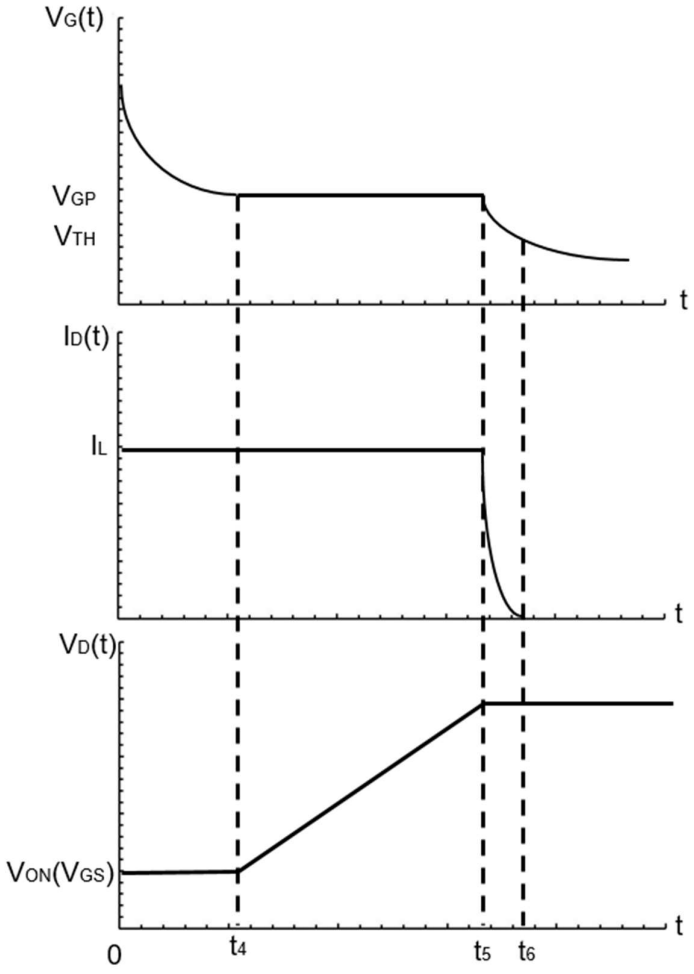


Figure 1.2-9 MOSFET V_{GS}, I_{DS} and V_{DS} transient waveforms at turn-OFF

Assuming that the gate drive has been triggered at time t_0, then the MOSFET V_{GS} is in exponential decay until time t_4. Between 0 and t_4, C_{GS} and C_{GD} are discharging through the negative gate current. The equation for this exponential decay in V_{GS} is given by (1,2-26) below.

$$V_{GS(t)} = V_{GG} e^{-\frac{t}{R_G(C_{GS}+C_{GD})}} \qquad (1.2\text{-}26)$$

As V_{GS} approaches V_{GP}, the discharge current is diverted to C_{GD} thereby causing V_{GS} to remain constant at V_{GP} since C_{GS} is no longer being discharged. The time period required for discharging C_{GD} determines the drain voltage commutation rate (dV_{DS}/dt). Based on equation (1,2-24), the drain voltage during the turn-OFF transient can be expressed using equation (1,2-27) below

$$V_{DS(t)} = V_{DSON} + \frac{(V_{GS}+V_{GP})t}{R_G C_{GDAV}} \qquad (1.2\text{-}27)$$

The drain voltage switching time ($t_5 - t_4$) can be calculated using equation (1,2-28) below

$$t_5 - t_4 = \frac{R_G C_{GDAV}}{V_{GP}}(V_{DS} - V_{DSON}) \qquad (1.2\text{-}28)$$

At the end of the Miller capacitance discharge duration at t_5, the MOSFET V_{GS} resumes its exponential fall to zero while the voltage across the MOSFET rises. As V_{GS} falls below V_{TH}, the drain current falls to zero. The current commutation time occurs between $V_{GS} = V_{GP}$ and $V_{GS} = V_{TH}$.

1.2.3. Device Conduction and Switching Losses

The switching losses of power MOSFETs depend on the parasitic capacitances and resistances. In hard switched power MOSFETs, there is simultaneously higher drain current and drain voltage during the switching transient, hence, the total switching energy increases with the duration of the switching transient. Since power MOSFETs are unipolar devices, then the switching durations are determined solely by the charging and discharging of parasitic capacitances as shown in the previous section. The average turn-ON and turn-OFF power losses of the power MOSFET can be expressed respectively using equation 1.2-29 and 1.2-30 below.

$$P_{SWON} = \frac{t_3 - t_1}{2T} I_L V_{DS} \qquad (1.2\text{-}29)$$

$$P_{SWOFF} = \frac{t_6 - t_4}{2T} I_L V_{DS} \qquad (1.2\text{-}30)$$

The conduction losses of a power MOSFET depend on the on-state resistance, which in turn depends on the voltage rating of the device. The conduction losses can be calculated from equation (1,2-31) shown below.

$$P_{ON} = \frac{t_{ON}}{T} I_L^2 R_{DSON} \qquad (1.2\text{-}31)$$

1.3. Silicon Carbide Technology

Silicon has been the work-horse of the semiconductor industry for both microelectronics for VLSI applications and power electronics for energy conversion applications. In both industries, silicon has been pushed to its limits although from different requirements. In the microelectronics industry, the need to miniaturize the physical length of the MOSFET has been the primary motivating factor leading to sub 50 nm CMOS technology

nodes. With gate oxides less than 1.5 nm and channel lengths of 22 nm, Moore's law has seen radical re-design of the MOSFET away from polysilicon gates to metal gates, silicon dioxide to high K dielectrics and planar MOSFETs to Fin-FETs. On the other hand, in power electronics, the need to improve power density, temperature management and reliability is also pushing silicon to its limits. Beyond 1.2 kV, silicon MOSFETs are simply not feasible using existing technologies. To the knowledge of the author, the only 1.2 kV silicon MOSFET commercially available from IXYS (with datasheet reference IXFN50N120SiC) exhibits very poor conduction and switching losses, it should be stated that the devices are of similar rating. Shown in Figure 1.14 are the measured turn-ON and turn-OFF losses of a 1.2 kV Si and SiC Power MOSFET. The SiC MOSFET is a 1.2 kV CREE MOSFET (with datasheet reference CMF10120D).

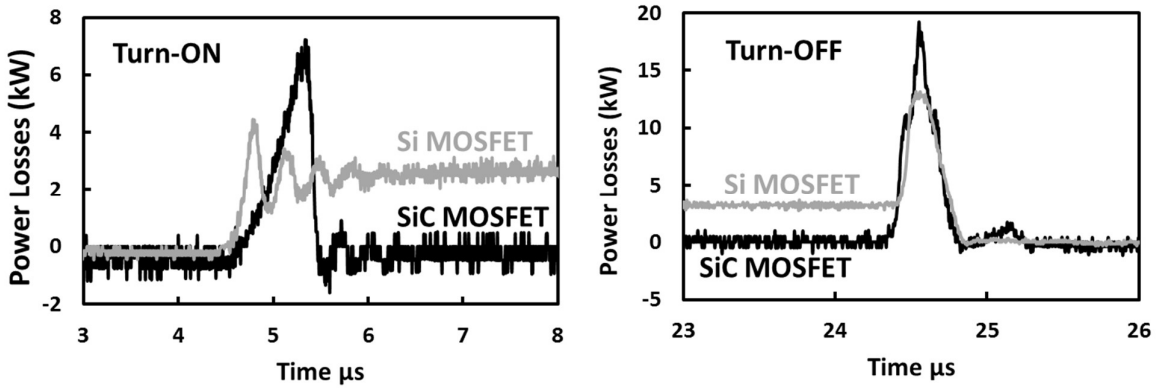


Figure 1.3-1 Turn-ON and Turn-OFF Power losses for a 1.2 kV Si and SiC MOSFET

The measurements in Figure 1.3-1 show very significant on-state losses in the Si MOSFET compared to the SiC power MOSFET (3 kW for silicon and 0.2 kW for SiC). The reason for the significantly reduced on-state losses for the SiC MOSFET is the wide bandgap characteristic of the technology.

SiC is a wide bandgap semiconductor with a bandgap of 3.3 eV which is approximately thrice that of silicon at 1.1 eV. It is an indirect bandgap semiconductor, which means that the valence band maximum and the conduction band minimum do not occur at the same wave

vector. Gallium nitride (GaN) is another wide bandgap semiconductor, however, given certain difficulties associated with GaN devices, they are not considered suitable for high voltage applications (above 1 kV). Due to the difficulties involved in growing bulk GaN substrates, GaN devices are usually lateral devices fabricated on foreign substrates like Si, SiC or Sapphire. Furthermore, the high channel mobilities achieved in GaN devices are based on 2-dimensional electron gas channels (2-DEG) resulting from the quantum wells formed in band discontinuities in AlGaN/GaN heterojunctions, hence, GaN devices cannot be made into vertical devices even if bulk substrates were made available. As a result, their current handling capabilities are not comparable to silicon or SiC power devices. Furthermore, coefficient of thermal expansion (CTE) mismatch between the GaN device and the foreign substrate reduces the reliability of GaN devices under power cycling. Reliable gate dielectrics are also difficult to implement on GaN devices which makes gate driving a challenge especially since they are usually depletion mode or normally off devices. For these reasons, this thesis focusses only on SiC power devices as a technology for high voltage power electronics.

The relationship between the intrinsic carrier concentration and the energy bandgap of a semiconductor is given by equation (1.3-1) below.

$$pn = n_i^2 = N_C N_V e^{-\frac{E_G}{K_B T}} \qquad (1.3\text{-}1)$$

The wide bandgap in SiC means that the intrinsic carrier concentration at a given temperature is low compared to silicon. This results from the fact that more thermal energy is required to generate electron hole pairs since the energy gap to be scaled in higher in SiC. The lower carrier concentration means SiC power devices are more robust at higher temperatures since the maximum temperature limit imposed on a semiconductor is determined by when the thermally generated carriers become more than the background doping. Hence, SiC is naturally a high temperature semiconductor. As a result of the wider bandgap, SiC has a higher critical electric

field compared to silicon, which means that a layer of SiC will block a higher voltage compared to a silicon layer. The critical electric field is the maximum field a semiconductor will sustain before under-going avalanche breakdown via impact ionization. The lower conduction losses demonstrated in the measurements of the 1.2 kV silicon and SiC MOSFETs presented in Figure 1.4 are a direct manifestation of the higher critical electric field in SiC compared with silicon. Hence, the voltage blocking drift layers of SiC MOSFETs are significantly more conductive than that of a silicon MOSFET designed to block the same voltage. SiC is also 8 times more thermally conductive than silicon and GaN, hence, heat transfer from the junction to the case in a SiC power device will occur more efficiently than a Si power device. This is important for enhancing electrothermal robustness under surge conditions like unclamped inductive switching. Figure 1.15 shows a comparison of SiC, silicon and GaN. As a result of these technical advantages, SiC power MOSFETs have been commercialized with voltage ratings at 600 V, 1.2 kV and 1.7 kV. The major manufacturers include Wolfspeed (formerly CREE) and ROHM. Other companies that have demonstrated SiC MOSFETs for in-house applications are Mitsubishi and GE. SiC power modules have also been released by CREE with 1.2 kV/150 A modules commercially available. A 1.2 kV/800 A SiC power module has also been demonstrated by researchers from oak-ridge national lab [7]. 10 kV and even 15 kV SiC MOSFETs have been demonstrated by researchers from CREE and used in various power system applications including power controllers and solid state transformers. Other demonstrators of SiC power devices have been compact solid state fault current limiters [8]and high voltage DC-DC converters for renewable power injection and control in micro-grids [9].

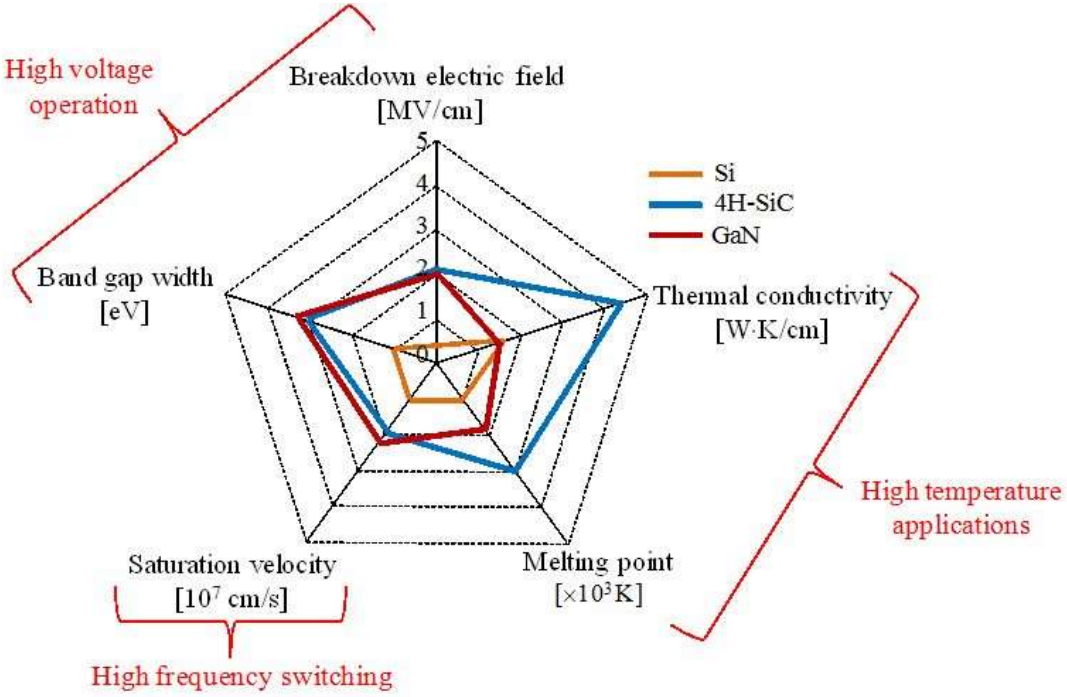


Figure 1.3-2 A Comparison of the Electrothermal Properties of Si, SiC and GaN

1.3.1. Silicon Carbide through the Years

The first scientist to suggest a chemical bond between Si and C was the Swedish chemist Jacob Berzelius [10] in 1824 however the first time large quantities of SiC became available for commercial use was in 1891 by Eugen Acheson [11]. Although he patented the procedure of making SiC, his initial goal was to manufacture diamond. Due to the extreme hardness of the material it was first used as an abrasive which remains an industrial use to this day. SiC is also widely used as a cutting material in the glass industry. The electronic use of the material came in subsequent years. Another usage of SiC was demonstrated by Colonel Henry Dunwood that used the material in radio receivers [12]. The first time SiC was used as semiconductor device was in 1955 when Jan Antony Lely in Philips managed to manufacture high grade crystal and saw the potential of the material as semiconductor [13]. The next big breakthrough came in 1978 when a new growth technique from Tsvetkov and Tairov was presented [14]. The first commercial supplier for SiC was CREE in 1987 and today, Wolfspeed

(formerly CREE) is one of the world leaders in the growth and fabrication of SiC power devices. The first high voltage SiC Schottky barrier diode was presented in 1992 from Bhatnagar. The diode was able to block 400V and the electrical superiority of SiC compared to Si immediately became evident [15]. The voltage blocking capabilities of SiC power devices started increasing with a 2 kV SiC power device demonstrated in 1994 [16] and Kordina et. al. [17] subsequently pushing the blocking voltage to 4.5 kV. The first commercially available SiC Schottky diodes emerged from CREE in 2001 with companies like Infineon, ROHM and Fairchild following suit. A major breakthrough happened in 2004 when Toyota in collaboration with Denso Corporation were able to produce substrates with massively decreased dislocations. This made the commercialization of SiC devices even more feasible. CREE at the time was also able to produce 100 mm SiC substrates and epitaxy material for commercial use. One of the major drawbacks of SiC is its increased cost compared to comparatively rated silicon devices. However, increased competition from industrial manufacturers of SiC power devices coupled with the increased availability of SiC wafers has put a downward pressure on the cost of the devices. The second major breakthrough in SiC was when the first MOSFET became commercially available in 2011. It was a 1.2 kV SiC MOSFET from CREE. After that first generation of MOSFETs, CREE developed subsequent generations of 1.2 kV SiC MOSFETs as well as 600 V and more recently, 1.7 kV devices.

2. Modeling Power Converters using Hard Switched Silicon Carbide MOSFETs and Schottky Barrier Diodes

2.1. Introduction

As stated earlier MOSFET are part of the unipolar device family because they use the majority carriers to conduct electricity. One on the major characteristics of any device is its V_{DS}-I_{DS} curve. It consists of 3 major regions. The first is the cut off region. It is where the gate voltage hasn't reached the required threshold voltage and the device is not conducting. Then there is the linear region where the drain source voltage is smaller than V_{GS}-V_{TH} and this the region in microelectronics where you can use the device as an amplifier. In power applications the devices are only used as switches so this region is not of any interest for power MOSFETs. And finally the third region is where the drain source voltage is larger than V_{GS}-V_{TH}. It is the saturation region and this is the on state in the power stage. A representation can be seen in the next figure

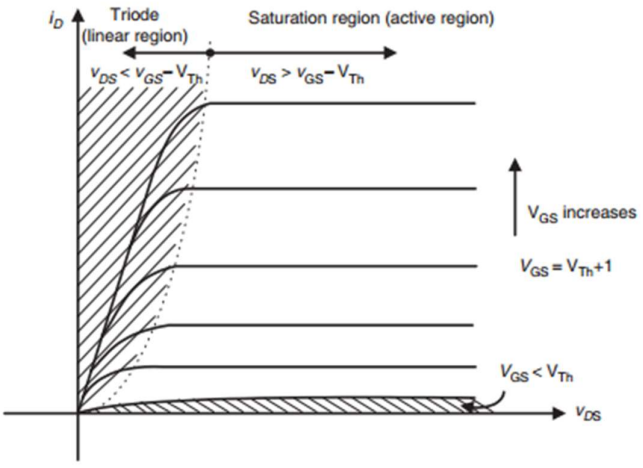


Figure 2.1-1 Vds-Ids Curves

As the gate source voltage increases so does the current through the device. It is evident that as the gate voltage increases the drain source voltage needs to be higher for the device to go into saturation mode. This is the reason the cornering point on every line is at a higher V_{DS}.

Another very important part in the structure of the device is capacitances of the device. There are three main capacitances that are created in between the junctions of a device. There is the gate source capacitance (G_{GS}), the gate drain capacitance (C_{GD}) and the drain source capacitance (C_{DS}). They are not linear and they depend on the device structure and geometry. Also the bias voltage is one of the main reasons they don't have a constant value. During the turn on of the device the two capacitances that are associated with the gate of the device need to be charged so the structure of the gate is of outmost importance. The value of them can be calculated from values that are given in the datasheet of the devices. The given values are the small signal reverse transfer capacitance (C_{rss}), the small signal input capacitance when the drain and the source of the device are sorted (C_{iss}) and the small signal output capacitance when the gate and the source are sorted (C_{oss}). A combination of the all three of them calculate the values of the capacitors [18]

$$C_{GD} = C_{rss} \quad (2.1\text{-}1)$$

$$C_{GS} = C_{iss} - C_{rss} \quad (2.1\text{-}2)$$

$$C_{DS} = C_{oss} - C_{rss} \quad (2.1\text{-}3)$$

2.2. Device operation region

As we stated earlier power devices are oprated at two of the three regions of the device. When the device is at cut off $V_{GS}<V_{TH}$ there is no channel formed on the device and there is no current flowing from the drain to the source. It is the off state of the switch. Then the device goes into the saturation region where $V_{GS}>V_{TH}$ a channel is formed and the device is conducting current from the drain to the source. The switch is in its on position. For the devices to work into these regions there are other restrictions also.

- For the saturation region the drain source voltage needs to be higher than the gate source minus the threshold voltage as well as the gate voltage higher than the threshold voltage
- For the cut off region the gate source voltage needs to be smaller than the threshold voltage of the device and the drain source voltage doesn't play any role.

This is so in normal operation. If the drain source voltage exceeds the breakdown voltage capabilities of the device than it will start conducting regardless of state of the gate. The need of a channel formation is not necessary in this case but details of that behavior of the device will be discussed in another chapter.

The drain current in the saturation region is

$$I_{DS} = K(V_{GS} - V_{TH})^2 \qquad (2.2\text{-}1)$$

Where: $K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)$ μ_n is the electron mobility, C_{ox} is the oxide capacitance, W is the width of the channel and L is the length of the channel. [18]

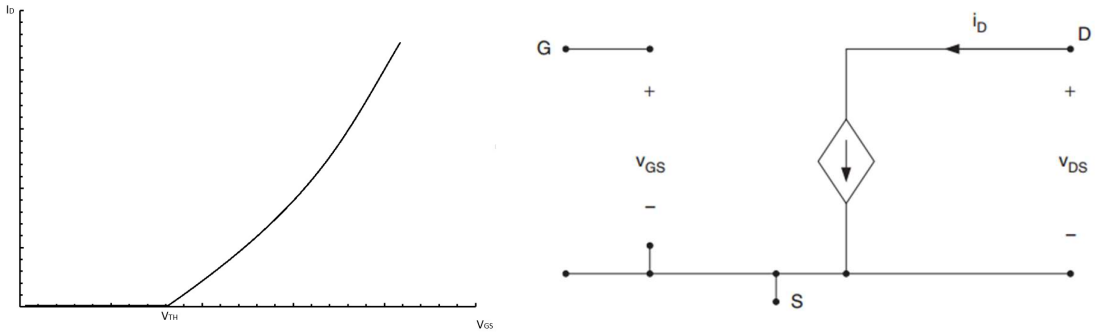


Figure 2.2-1 Threshold voltage and equivalent circuit

2.3. Basic Device models using equivalent circuits

There are models that try to predict the behavior of a power device with the use of equivalent circuits. One of the difficult part to simulate as stated earlier is that the intrinsic capacitances

of the device do not stay constant as the drain source voltage changes. An example is presented for 900V SiC MOSFET in Figure 2.3-1

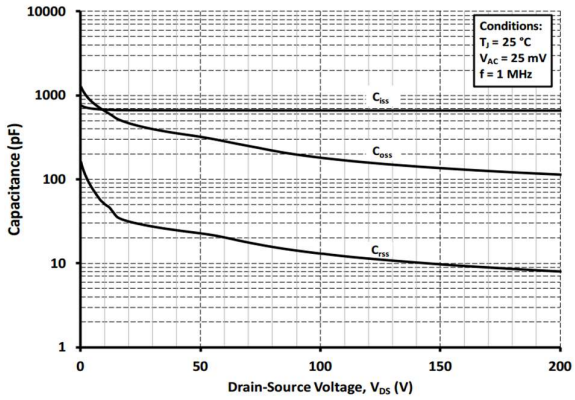


Figure 2.3-1 Device Capacitances-Vds [6]

When using equivalent circuits the best solution is to use approximations. It will induce an error to the results but careful selection will give reasonably good results.

The most common equivalent circuit will be presented. The device drives an inductive load and parallel to the load there is a diode to circulate the current when the device is in off state. The device characteristics that are used as input of the device model are the gate resistance R_G, The gate drain capacitance C_{GD}, and the gate source capacitance C_{GS}. The circuit can be seen in Figure 2.3-2

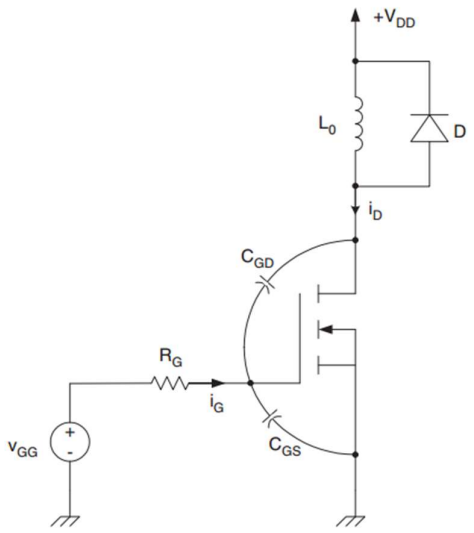


Figure 2.3-2 Simple Equivalent circuit

A better way to understand how the device behaves is to create an equivalent circuit for each of the time stages the device goes through both for turn on and turn off.

2.3.1. Simplified switching equivalent circuits

As explained in the introduction there are four phases. [19]

- Phase 1: $t_o < t < t_1$, $V_{GS} < V_{TH}$
- Phase 2: $t_1 < t < t_2$, $V_{GS} > V_{TH}$, $I_{DS} < I_o$
- Phase 3: $t_2 < t < t_3$, $V_{GS} > V_{TH}$, $I_{DS} = I_o$
- Phase 4: $t_3 < t < t_4$, $V_{GS} > V_{TH}$, $I_{DS} = I_o$, C_{GD}, C_{GS} *charged*

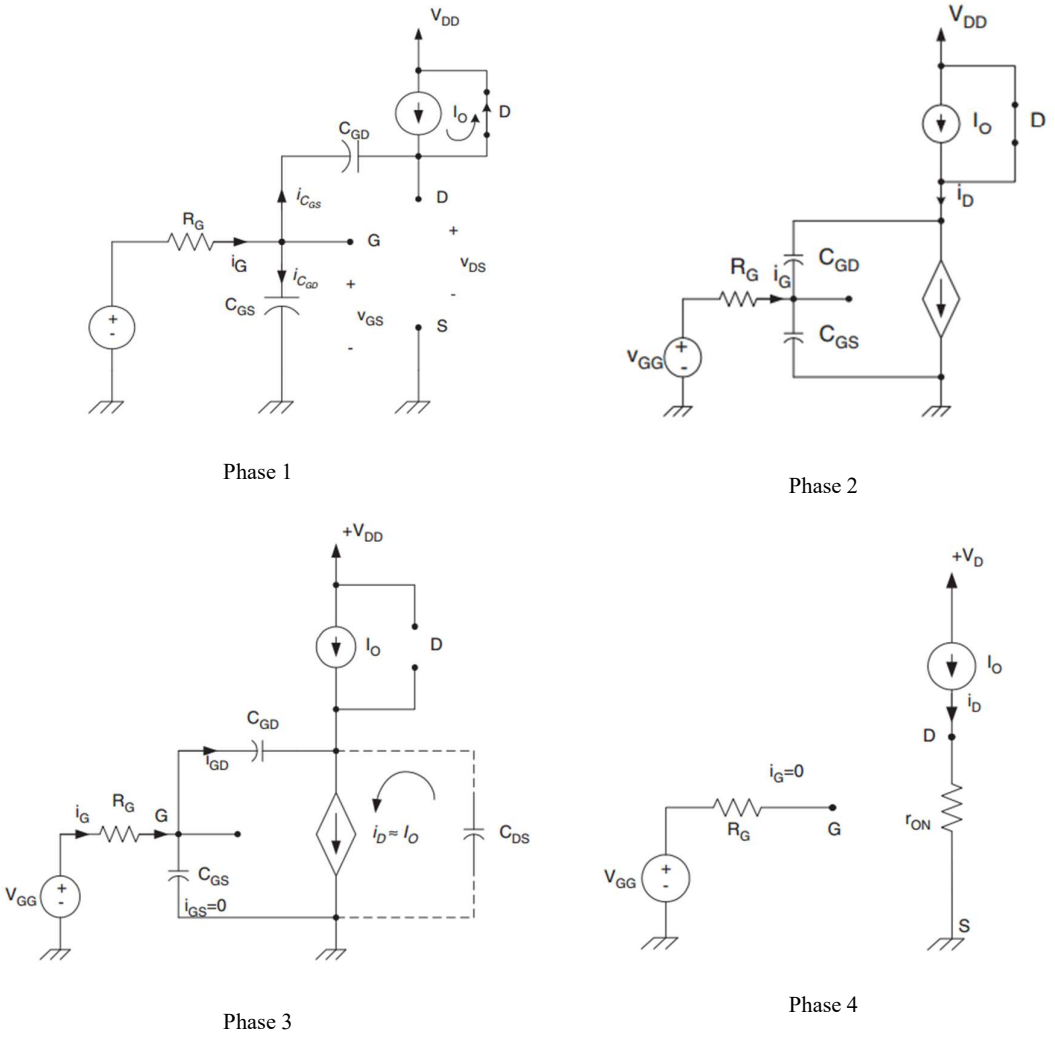
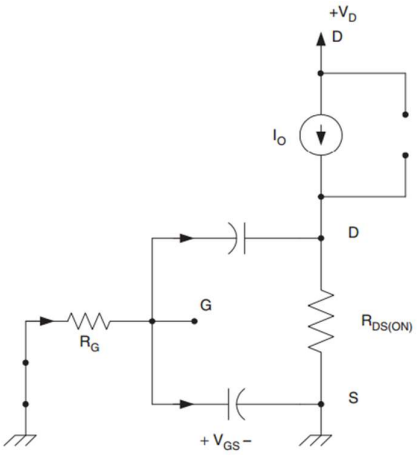


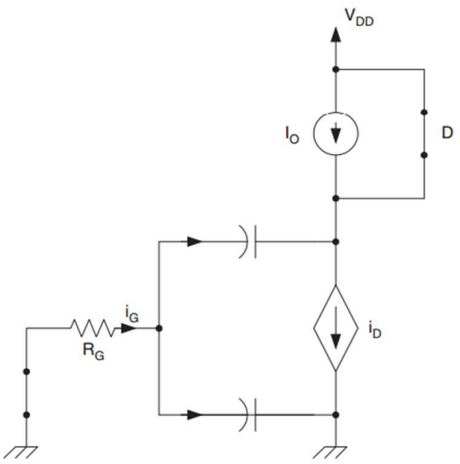
Figure 2.3-3 Turn on equivalent circuits

Similarly there are four phases for the turn off of the device

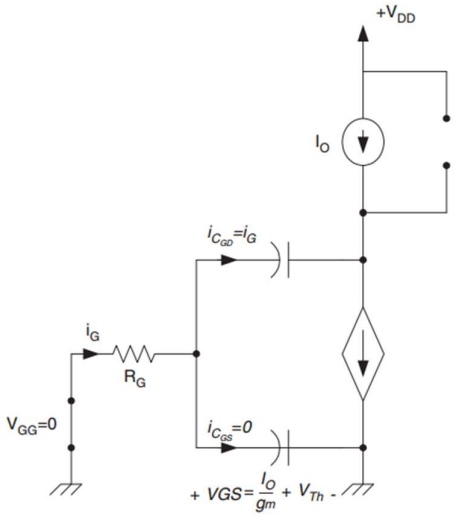
- Phase 1: $t_o < t < t_4,\ V_{GS} < V_{GP}$
- Phase 2: $t_4 < t < t_5,\ V_{GS} = V_{GP}, V_D > V_{ON}$
- Phase 3: $t_5 < t < t_6,\ V_{GS} < V_{GP}, V_D > V_{ON}, I_{DS}$ *Decreasing*
- Phase 3: $t_6 < t,\ V_{GS} = V_{TH}, V_D = V_{DD}, I_{DS} = 0$



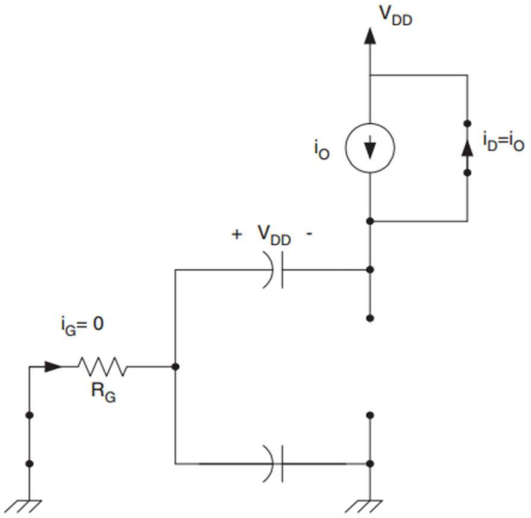
Phase 1



Phase 2



Phase 3



Phase 4

Figure 2.3-4 Turn off Equivalent Circuits

2.4.Device Modelling Strategies and their importance

The emergence of silicon carbide MOSFETs and Schottky Barrier Diodes (SBD) at higher voltage and current ratings is opening up new possibilities in the design of energy dense power converters. However, packaging constraints like parasitic inductances limit how fast the MOSFETs and diodes can switch, because of high frequency electromagnetic oscillations or ringing. Ringing is a reliability concern as it stresses the devices and causes additional losses to the switching losses. It has been documented that excessive ringing can even result in the parasitic turn on off an H-Bridge lower device when the upper device is on due to high dI/dt which is sufficient to turn on the gate. In a half bridge when the upper device is on the lower device needs to be off. A this state the voltage can be expressed:

$$V_{GS} = \frac{C_{GD}}{C_{GD}+C_{GS}} V_{DS} \qquad (2.4\text{-}1)$$

Even if the voltage from the gate driver is set to zero there is a possibility the device might turn on due to the change in the drain-source voltage and the voltage divider consisting of the gate drain capacitance and the gate source capacitance. Because of the nature of this voltage divider it can react really fast on all the transients between the drain and the source. This phenomenon becomes even more prominent in higher frequencies.

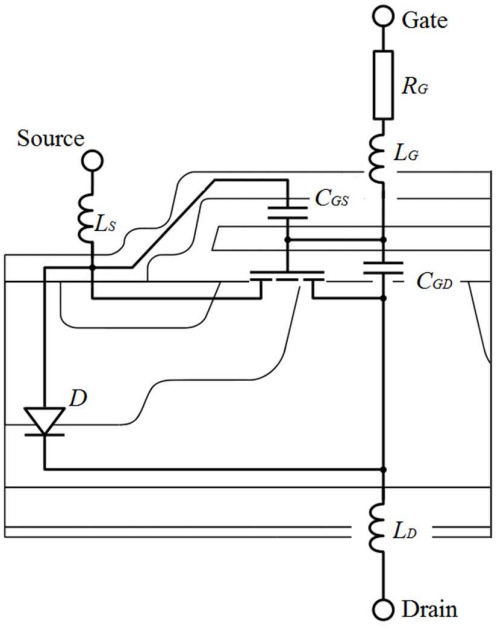


Figure 2.4-1 Parasitic Elements in a power MOSFET

However, the fast switching output transients (dI_{DS}/dt and dV_{DS}/dt) coupled with parasitic capacitances and inductances from the package or module, cause electromagnetic instability in the form of ringing. This is a reliability concern from the point of view of increased losses and electromagnetic interference. Furthermore, excessive ringing may take the device beyond its rated capacity. For wide bandgap devices it is not uncommon to have voltage spikes 100% higher than the drain source voltage applied to the device. Due to their ability to switch on very fast compared to conventional Si MOSFETs it is very common to be used in hard switching applications. That extenuates the phenomenon and the solution is to reduce the dV/dt, making the switching softer, The way to control this phenomenon is by either reducing the switching frequency or use snubbers to dampen this behavior. Solutions like these are not acceptable for a number of applications because you lose the benefits of using devices that can change state very fast. The reason this excessive ringing happens is due to the parasitic elements that are intrinsic in a device. Figure 2.4-1 shows a number of them. The problem becomes even bigger if we take into consideration all the parasitics that are added due to the PCB manufacturing. Hence, it is important to be able to accurately model and characterize the additional power

losses and terminal instability that arise from fast switching transients in the presence of parasitics. Early MOSFET and diode switching models did not take into account the parasitic inductances, hence could not distinguish the ringing from fast switching. Subsequent models took into consideration the source and drain inductances and were implemented in the time domain, which yielded mathematical expressions that do not lend easy use. If these equations were made simpler the accuracy of their findings would be a lot smaller. Models that take into account the dynamic characteristics of the device can be incorporated into this type of models. Ringing behavior of the MOSFET is not easy to represent in the time domain [20]. In the model developed in [21], the gate, source and drain inductances have been taken into account. However, because the model was developed for low voltage MOSFETs with shorter switching transients, the effects of the parasitic elements are less pronounced. Also the switching waveforms do not show any oscillations, therefore ringing losses are not considered. As the switching frequency is increased with higher voltage/current ratings these cannot be neglected. In [22], switching transient analysis have been performed on a MOSFET with a free-wheeling diode and a snubber, however, there was no consideration of ringing or oscillations. Furthermore, the use of snubbers can counteract against the fast switching benefits that SiC unipolar devices deliver as stated earlier. In [23], the source and drain inductances have been taken into account as well as the non-linearity of the parasitic capacitors. In [24], the switching characteristics of SiC Schottky diodes are compared with silicon PiN diodes and it is shown that ringing occurs for the SiC diode and can contribute to the total switching losses. In literature there have been attempts to model the dynamic behavior of capacitances of the devices using SPICE equivalent models to simulate the transient and validate the mathematical expressions derived for the capacitances. Mathematical expressions have been populated for the different switching stages of the device [25]. Issues arising from the device capacitance are even more important when the device will be used in applications the device is required to

switch at high frequencies. Accurate mathematical expressions become a lot more difficult and the low switching models are not accurate enough. SABER is also used in this kind of modelling to get the needed accuracy and not to be computationally very demanding [26]. Other modelling approaches are extracting numerical values from experimental data and validating them with similar type experiments. Temperature dependencies can be added to the calculations to make them more complete. Methods like this are very handy for practical implementation of the models but lack accuracy and they cannot be applied to any kind of application because they are very much dependant on the structure of the circuit as well as the type of device that is used [27]. The importance of the structure of the drift region of the device as well as the channel have also been modelled. Having a mathematical representation of both of them can help us understand how a device behaves and how important role the parasitics play on the device behaviour [28]. The goal is to make a mathematical representation of the device switching that would fast and easy be able to calculate the switching behaviour of both SiC MOSFETs and SiC Schottky Diodes. It is important to be able to model both the behaviour of these devices because in applications most inverter or converter applications an antiparallel diode is always connected to the device. Being able to model them at the same time gives an advantage when considering the whole system. The characterization was done using different gate resistors so we are able to emulate that element also. All parasitic elements -gate, source and drain inductances- have been considered and actual ringing has been modelled. The model accounts for current commutation between the diode and the MOSFET and analyses the impact of ringing on the power losses. The parasitic inductances and capacitances of the diode have also been incorporated. The model is developed and implemented in the frequency domain using MATLAB SIMULINK and is compared to experimental measurements of CREE SiC MOSFET (CMF20120D) and diodes rated at 1.2 kV. Later on the model for both the MOSFET and the diode will be described, a comparison with the experimental results will be presented

and at the end of the chapter a conclusion will be derived about the validity of the model how well it matches to the experimental results.

2.5. Model Derivation

The terminal voltage and current switching characteristics of the MOSFET and the diode are developed as a first principle. All parasitics including the gate (L_G), source (L_S) and drain inductances (L_D), as well as the gate-source (C_{GS}) and gate-drain (C_{GD}) capacitances are taken into consideration.

2.5.1. MOSFET Model

The classical gate charging characteristic shown in Figure 2.5-1 are considered, where the gate voltage of a typical MOSFET is shown as a function of time. Figure 2.5-1 the gate-source voltage (V_{GS}) increases exponentially as the gate-source capacitor is charged between time t_0 and t_1. Between t_1 and t_2, the drain current (I_{DS}) increases and V_{GS} approaches the plateau voltage, which is when the gate-drain capacitance starts charging i.e. Miller effect. Between t_2 and t_3, the drain-source voltage (V_{DS}) collapses from the off-state blocking voltage to the on-state voltage which depends on the on-state resistance (R_{DSON}) and the forward current (I_{DS}). After C_{GD} has fully charged, V_{GS} resumes its exponential rise to the gate-drive voltage which is between time t_3 and t_4.

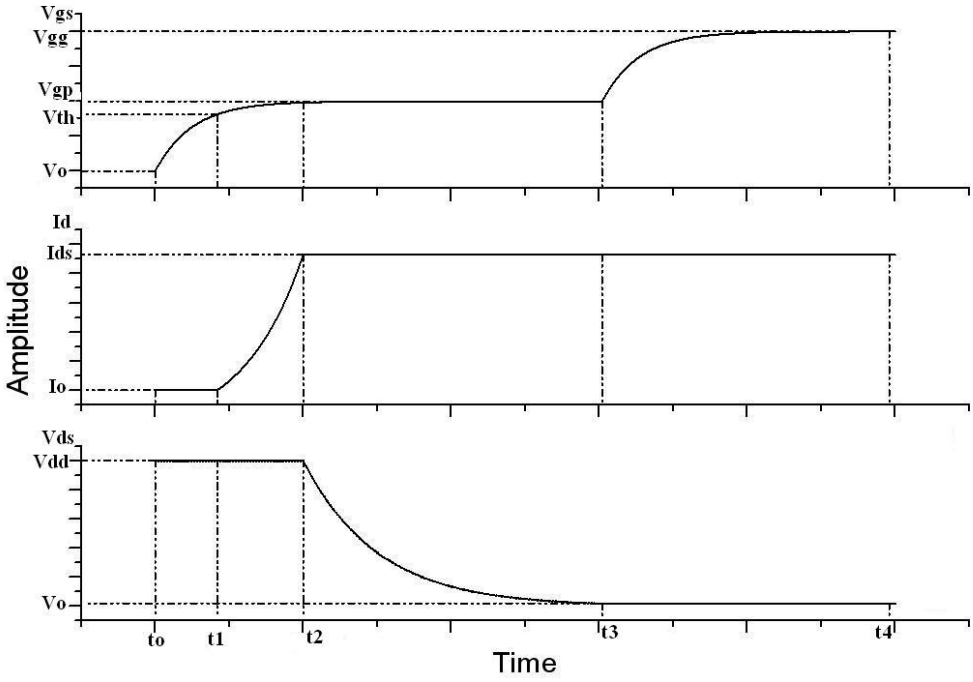


Figure 2.5-1 Ideal turn-on characteristics for V_{GS}, I_D and V_{DS} respectively

Figure 2.5-2 shows the experimental switching waveforms measured from 1200V/30A SiC MOSFETs (CMF20120D from CREE) where oscillations can be observed in the V_{DS}, V_{GS} and I_{DS} characteristics. Because the characteristics in Figure 2.5-1 do not account for parasitic inductances, they are unable to capture oscillations in the device and will not be accurate in the calculation of switching losses or the prediction of ringing losses.

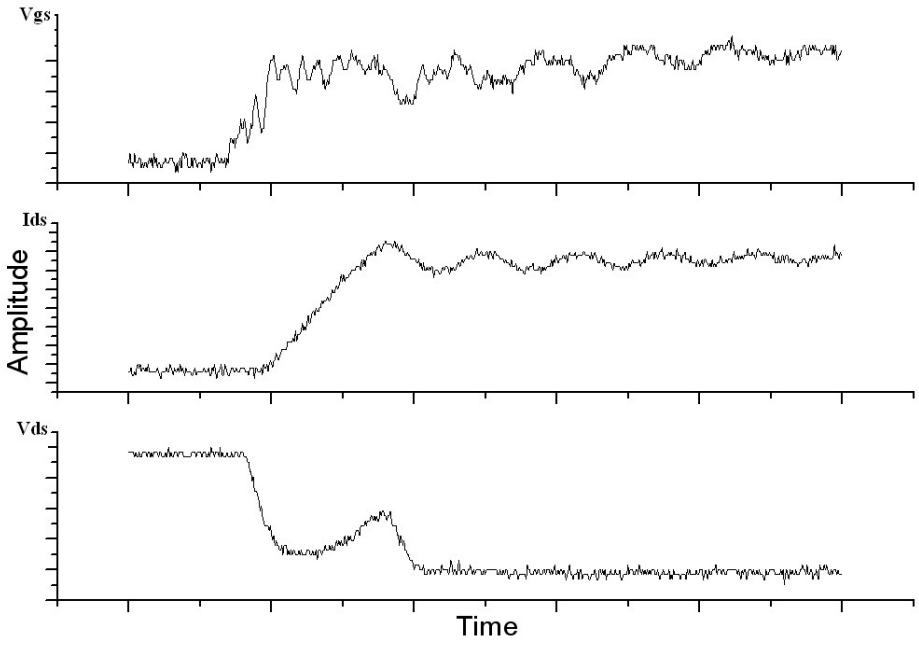


Figure 2.5-2 Measured turn-on graphs for V_{GS}, I_D and V_{DS} respectively

To overcome this limitation and to more accurately model switching and ringing losses, different techniques that take parasitic inductances into account have been presented. In [29, 30] SPICE was used for modelling the transients, SPICE model can give quite accurate result but it is computationally impossible to simulate the devices for a long period of time. When a system model it is necessary to incorporate solutions that are a lot faster even in a expense of accuracy. Other issues that arise when using SPICE modelling is the way this models are populated from device manufacturers. The values required to describe the devices are generated automatically and they are based in already existing Si technology. Except the difference in material the type of device that resembles the power handling capabilities of the MOSFET are the IGBTs so the models have to be based on them. The device structure is very different though and also the dependence of the R_{DSON} from temperature as well as the threshold voltage in SiC is the exact opposite than Si. Consequently creating a SiC MOSFET model is not without its challenges[31]. Using SABER is the most accurate tool to capture the ringing. Again the computational power required is quite high and when longer simulation periods are necessary

or variable conditions need to be incorporated to the model another approach is necessary [32] in [33], time domain mathematical models were used, a solution that over comes the restrains from the other two. The problem with using time domain equations are they are bulky and generally difficult to handle. In this chapter the use of the frequency domain was utilized. It is a lot easier to extrapolate the equations and with the use of system modelling tools in MATLAB it is easy to model how the system will behave in any type of input. In this case, the MOSFET switching transients will be simulated for the different time frames i.e. V_{GS} changing (C_{GS} charging/discharging) and V_{DS} changing (C_{GD} charging/discharging).

2.5.2. From t_0 to t_1

Figure 2.5-3 shows the equivalent circuit of the MOSFET during this phase of switching when C_{GS} is charging and V_{GS} is below the threshold voltage.

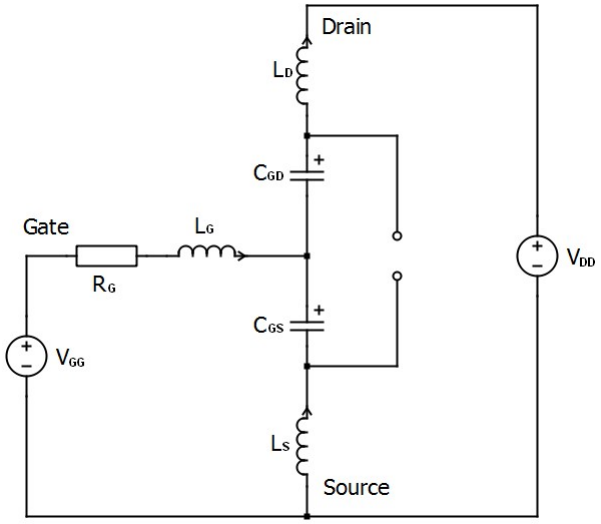


Figure 2.5-3 Equivalent circuits for the MOSFET from t_0 to t_1

The following equations are derived by applying basic nodal analysis to the terminals of the MOSFET in the equivalent circuit

$$(V_D - V_G)sC_{GD} + \left(\frac{V_D - V_{DD}}{sL_D}\right) = 0 \qquad (2.5\text{-}1)$$

$$(V_G - V_S)sC_{GS} + \left(\frac{V_G - V_{GG}}{R_G + sL_G}\right) + (V_G - V_D)sC_{GD} = 0 \qquad (2.5\text{-}2)$$

$$(V_S - V_G)sC_{GS} + \frac{V_S}{sL_S} = 0 \qquad (2.5\text{-}3)$$

V_{GS} is derived from these equations:

$$V_{GS} = \frac{As^2 - V_{DD} + V_{GG}}{A_1 s^4 + B_1 s^3 + C_1 s^2 + D_1 s + 1} \quad (2.5\text{-}4)$$

Where:

$$A = C_{GD}\, L_D\, V_{GG} - C_{GD}\, L_D\, V_{DD}$$

$$A_1 = C_{GD}C_{GS}L_G L_D + C_{GD}C_{GS}L_D L_S + C_{GD}C_{GS}L_G L_S$$

$$B_1 = C_{GS}C_{GD}L_G R_G + C_{GD}L_S C_{GS}R_G$$

$$C_1 = C_{GD}L_D + C_{GD}L_G + C_{GS}L_G + C_{GS}L_S$$

$$D_1 = C_{GD}R_G + C_{GS}R_G$$

2.5.3. From t_2 to t_3

The equivalent circuit for this phase of operation is shown in Figure 2.5-4

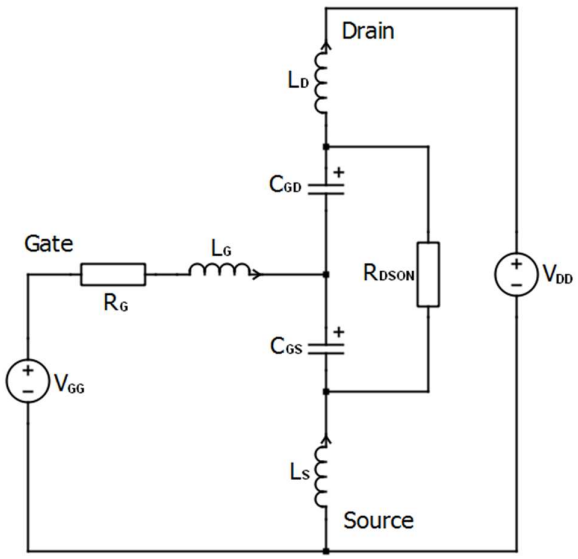


Figure 2.5-4 Equivalent circuits for the MOSFET from t_2 to t_4

During this time frame V_{GS} is constant and V_{DS} is changing due to the Miller effect. Using the same nodal analysis, the following equations are derived for V_{DS}

$$(V_D - V_G)sC_{GD} + \left(\frac{V_D - V_{DD}}{sL_D}\right) + \left(\frac{V_D - V_S}{R_{DSON}}\right) = 0 \quad (2.5\text{-}5)$$

$$(V_G - V_S)sC_{GS} + \left(\frac{V_G - V_{GG}}{R_G + sL_G}\right) + (V_G - V_D)sC_{GD} = 0 \quad (2.5\text{-}6)$$

$$(V_S - V_G)sC_{GS} + \left(\frac{V_S - V_D}{R_{DSON}}\right) + \frac{V_S}{sL_S} = 0 \quad (2.5\text{-}7)$$

V_{DS} is derived from these equations:

$$V_{DS} = \frac{K}{(sR_GC_{GD}+1)} \frac{A_2s^2 + B_2s + R_{DSON}V_{DD}}{A_3s^4 + B_3s^3 + C_3s^2 + D_3s + R_{DSON}} \quad (2.5\text{-}8)$$

Where:

$$A_2 = C_{GD}L_GR_{DSON}V_{DD} + C_{GD}L_DR_{DSON}V_{GG} + C_{GS}L_GR_{DSON}V_{DD} + C_{GS}L_SR_{DSON}V_{DD} - C_{GS}L_SR_{DSON}V_{GG}$$

$$B_2 = C_{GD}R_{DSON}R_GV_{DD} + C_{GS}R_GR_{DSON}V_{DD}$$

$$A_3 = C_{GD}C_{GS}L_GR_{DSON}L_S + C_{GD}C_{GS}L_GL_SR_{DSON}$$

$$B_3 = C_{GD}L_GL_D + C_{GS}L_DL_G + C_{GD}L_GL_S + C_{GS}L_DL_S + C_{GD}L_GL_S + C_{GS}L_GL_S + C_{GD}C_{GS}L_DR_{DSON}R_G + C_{GD}C_{GS}L_SR_{DSON}R_G$$

$$C_3 = C_{GD}L_DR_{DSON} + C_{GD}L_DR_G + C_{GS}L_DR_G + C_{GD}L_GR_{DSON} + C_{GS}L_GR_{DSON} + C_{GS}L_SR_{DSON} + C_{GD}L_SR_G + C_{GS}L_SR_G$$

$$D_3 = L_D + L_S + C_{GD}R_{DSON}R_G + C_{GS}R_{DSON}R_G$$

2.6.DIODE model

Similar principles have been adopted for modelling the transient characteristics of the diode. The diode can be modelled as a stray inductance, voltage dependent depletion capacitance and a parasitic series resistance as shown in Figure 2.6-1 [24].

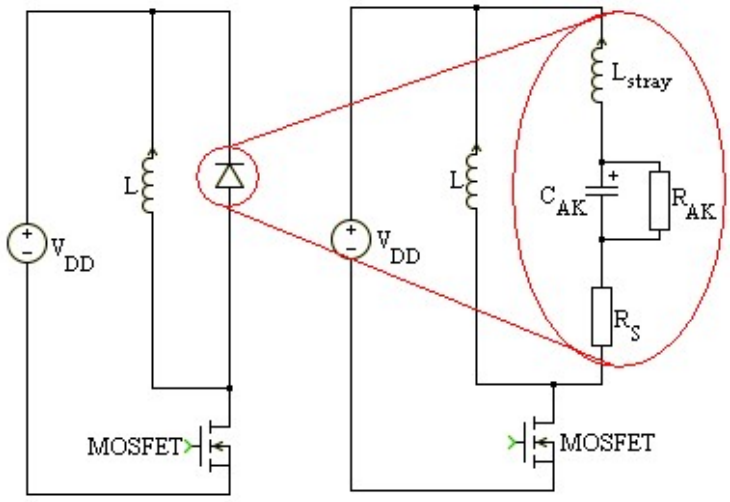


Figure 2.6-1 Clamped inductive switching test rig and equivalent circuit showing the diode parasitics

The equation for the diode transients can be developed from the transfer function of the diode equivalent circuit and the input voltage

$$V_{AK} = \frac{V_{DD}}{(sR_GC_{GD}+1)} \frac{\frac{R_S+R_{AK}}{R_{AK}L_{stray}C_{AK}}}{s^2+\left(\frac{R_SR_{AK}C_{AK}+L_{stray}}{R_{AK}L_{stray}C_{AK}}\right)s+\frac{R_S+R_{AK}}{R_{AK}L_{stray}C_{AK}}} \quad (2.6\text{-}1)$$

The transfer function of the diode equivalent circuit is also used to model the electrical current commutation between the diode and the MOSFET the difference is the value used for R_S. The input signal that was used was step input with custom low and high signals. Due to the importance of the gate resistance on how fast the device will switch a small delay on how the input of the step input will behave was added that is dependent on the gate resistance used.

2.7. Electro-thermal model for Bipolar latch-up

In this section a model has been created to calculate the junction temperature of a MOSFET during avalanche. The mechanism that forces the device to go into avalanche is explained in a later chapter. The model uses an electrical input to calculate the temperature which in turn is used to estimate temperature-dependent MOSFET parameters[34]. These MOSFET parameters (body voltage drop and in-built body potential) determine whether or not the

parasitic bipolar has latched. If the latch up occurs the device will fail due to avalanche. The output is then fed back into the temperature model in a cyclical process. The model is based on an inductor forcing current through the MOSFET from the drain to the source and assumes that the inductor has been pre-charged to a defined current. Equation $I_{(t)} = I_{AV} - \frac{V_{(t)}}{L}$ (2.7-1) below describes the current flowing through the MOSFET

$$I_{(t)} = I_{AV} - \frac{V_{(t)}}{L} \quad (2.7\text{-}1)$$

Where I_{AV} is the peak avalanche current, *I(t)* is the current flowing through the MOSFET, *V(t)* is the voltage across the MOSFET, *L* is the value of the inductor and *t* is time. The avalanche current is the peak current and depends on how much current is initially stored in the magnetic field of the inductor. The inductance determines the peak value of the avalanche current together with the charging duration. The current determined from $I_{(t)} = I_{AV} - \frac{V_{(t)}}{L}$ (2.7-1) is used to calculate the junction temperature of the MOSFET using the equation below

$$T_{(t)} = T_{AMB} + R_{TH} I_{(t)} V_{(t)} \left(1 - e^{-\frac{t}{R_{TH} C_{TH}}}\right) \quad (2.7\text{-}2)$$

Where *T(t)* is the junction temperature of the MOSFET, T_{AMB} is the ambient temperature, R_{TH} is the thermal resistance of the MOSFET and C_{TH} is the thermal capacitance of the MOSFET. The calculated junction temperature in $T_{(t)} = T_{AMB} + R_{TH} I_{(t)} V_{(t)} \left(1 - e^{-\frac{t}{R_{TH} C_{TH}}}\right)$ (2.7-2) $I(t) = I_{AV} - \frac{V_{(t)}}{L}$ (2.7-1)is used to calculate the built-in source to body pn junction potential using the equation below [35]

$$\Phi_{bi} = \frac{K_B T_{(t)}}{q} ln\left(\frac{N_E N_B}{n_i^2}\right) \quad (2.7\text{-}3)$$

where Φ_{bi} is the built in junction voltage of the parasitic BJT, K_B is the Boltzmann constant, *q* is the electric charge, N_E is the emitter (source) doping of the parasitic BJT (MOSFET), N_B is the base (body) doping of the parasitic BJT (MOSFET) and n_i is the intrinsic carrier concentration. The intrinsic carrier concentration has a temperature dependency that is material

dependent and is different for silicon and SiC. Since SiC has a wider band-gap it will have a lower intrinsic carrier concentration, hence a higher built-in junction voltage (Φ_{bi}). For example, at 300 K SiC has an intrinsic carrier concentration of 1.5x10-8 cm-3 whereas it is 1.5 x 1010 cm-3 for silicon. As a result, the built-in junction voltage for 4H-SiC will be approximately 3 times that of silicon[35]. As a consequence, the parasitic BJT will be harder to turn-on in SiC since a greater voltage is needed to forward bias the emitter-base junction. The body resistance of the MOSFET is calculated using the equation below

$$R_{PB} = \frac{l}{AN_B q \mu_P} = \frac{l}{AN_B q \cdot \left(\frac{T}{300}\right)^{-2.2}} \qquad (2.7\text{-}4)$$

Where l is the length, A is the area and μP is the hole mobility [35]. The voltage drop across the body resistance is calculated using the equations below

$$V_{PB} = \frac{I_C}{\beta} R_{PB} \qquad (2.7\text{-}5)$$

Where I_C is the collector current of the parasitic BJT and β is the gain of the BJT. The condition for bipolar latch-up is set by comparing V_{PB} to Φ_{bi}. The parasitic bipolar latches when $V_{PB} > \Phi_{bi}$. In this case, the current through the MOSFET is calculated using the equation below, which is originally derived for BJTs [35].

$$I_{(t)} = qA \frac{D_B n_i^2}{W_B N_B} \left(e^{q \frac{V_{FB} - \Phi_{bi}}{K_B T}} - 1 \right) \qquad (2.7\text{-}6)$$

If $V_{PB} < \Phi_{bi}$ the parasitic bipolar does not latch and the current through the MOSFET is determined by $I_{(t)} = I_{AV} - \frac{V_{(t)}}{L}$ (2.7-1). Figure 2.7-1 shows a schematic diagram illustrating how the electro-thermal model works.

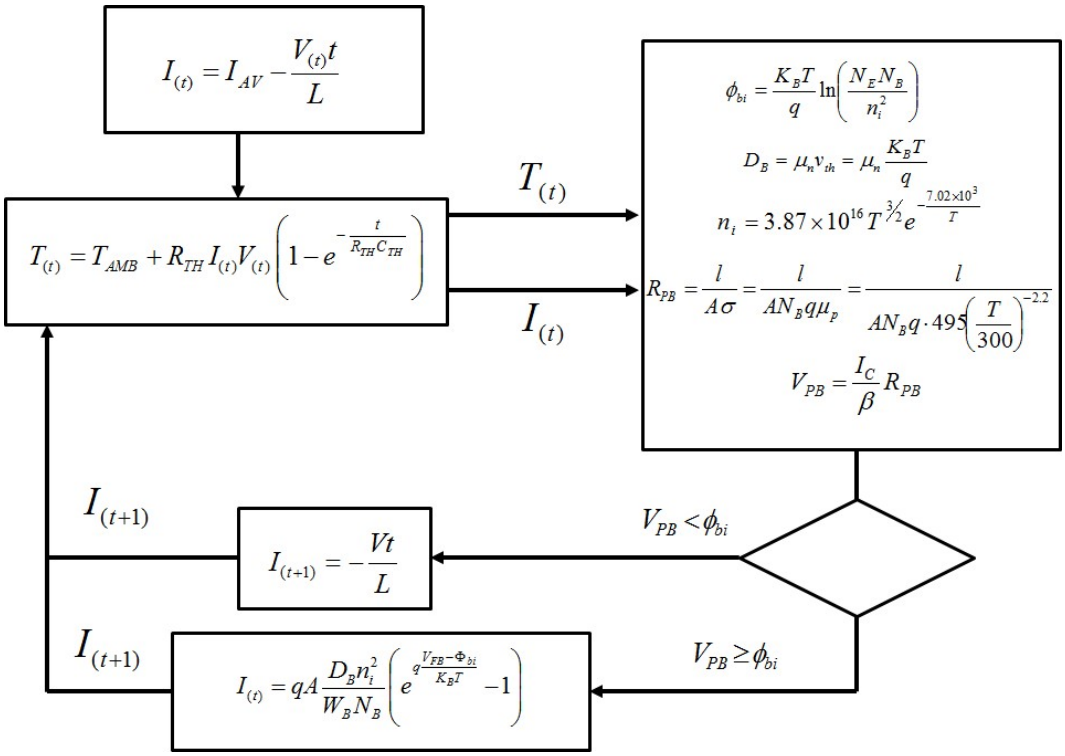


Figure 2.7-1 Electro-thermal model for parasitic BJT latch-up for MOSFET in avalanche

Figure 2.7-2 shows the trend of calculated normalized currents using the model in Figure 2.7-1 at different ambient temperatures. Figure 2.7-2 and Figure 2.7-3 illustrates that the parasitic bipolar latches for higher ambient temperatures but this is not the case for lower ones. Due to latching up the device will fail or significant damage will occur.

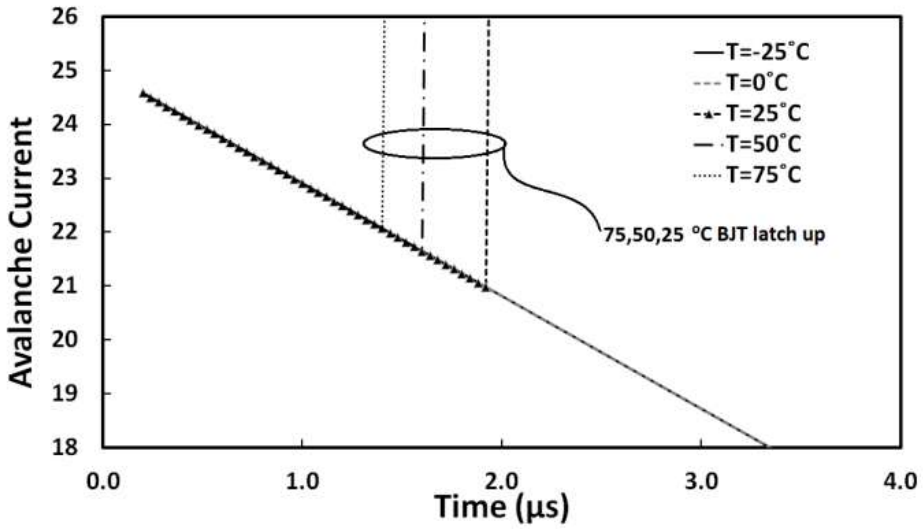


Figure 2.7-2 calculated device current as a function of time at different ambient temperatures

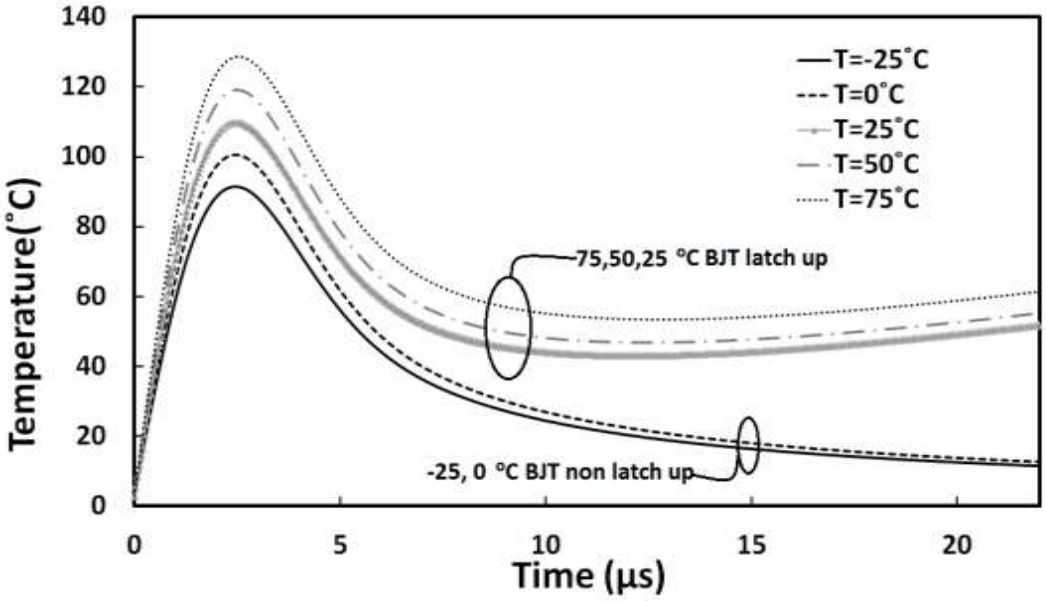


Figure 2.7-3 Calculated junction temperature as a function of time at different ambient temperatures

The process of latching is characterized by a rising current, which in reality will be limited by the power supply as will be demonstrated experimentally later on. Figure 2.7-3 shows the calculated junction temperature of the MOSFET obtained from Figure 2.7-1. It can be seen in Figure 2.7-3 that there is a temperature rise resulting from the peak avalanche power. However, for the case of latch-up there is a subsequent temperature rise during the cooling period which is due to the rising current from the activation of the parasitic BJT [34-39]. With detailed knowledge of device dimensions and process parameters, the calculations in Figure 2.7-2 and Figure 2.7-3 can be used by the designer as a predictor of BJT latch up for a specific device.

2.8. Experimental results

2.8.1. Set up & Measurements

The experimental set up can be seen in Figure 2.8-1 and the circuit diagram in Figure 2.8-2. The devices used were CREE SiC 1200V/33A MOSFETs and the diode was an Infineon 200A

SiC diode. The circuitry consists of a half bridge with the two MOSFETs in parallel and one diode

Figure 2.8-1Experimental test rig and environmental chamber-Measuring equipment

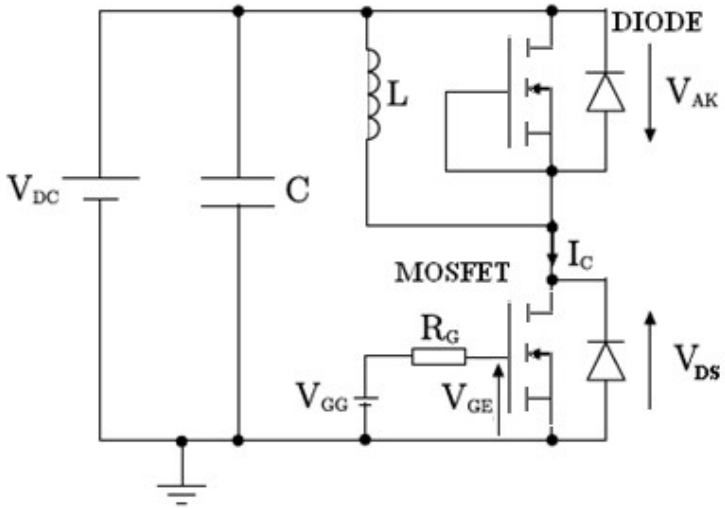


Figure 2.8-2 Circuit Diagram for testing rig

The freewheeling diode was connected across an 800 µH inductor. The supply voltage (V_{DD}) was set to 200 V and the gate drive voltage (V_{GG}) was set to 18V. The gate was connected to a Tektronix AFFG3022 signal generator through an optocoupler (HCPL 3120) for protecting the pulse generator from any power surges. The results were taken from a Tektronix TDS5054 digital oscilloscope and the static characteristics of the devices were measured by a Tektronix curve tracer. The current through the device was measured with the digital oscilloscope through a Tektronix TCP303 current probe.

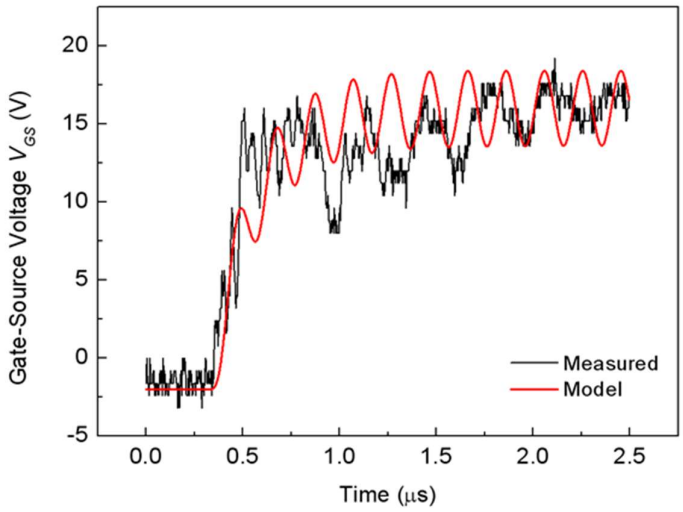


Figure 2.8-3 Measured and modelled V_{GS} characteristics for R_G of 22Ω

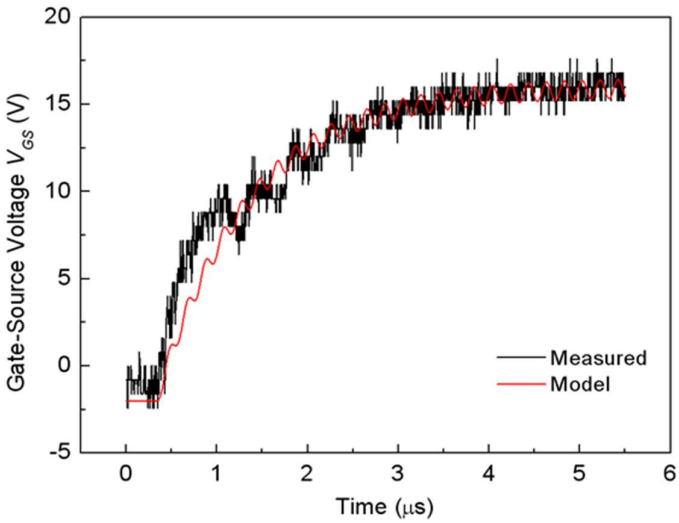


Figure 2.8-4 Measured and modelled V_{GS} characteristics for R_G of 100Ω

As the MOSFET switches ON, V_{GS} rises from zero to the gate-drive voltage (V_{GG}) and V_{DS} falls from the supply voltage (V_{DD}) to the on-state voltage. Also, the free-wheeling diode voltage (V_{AK}) rises from the on-state voltage drop to V_{DD}. The current, initially free-wheeling through the diode starts diverting into the MOSFET. Figure 2.8-3 compares the experimentally measured V_{GS} turn-ON transient with the simulated transient when switched with a gate resistance (R_G) of 22 Ω. Figure 2.8-4 shows the same comparison when switched with an R_G of 100 Ω. To obtain similar characteristics, values of the parasitic inductances have been varied typically between tens of nH and a few μH. The diode and MOSFET parasitic inductances (L_G,

L_S, L_D and L_{stray}) affecting the measurements not only result from the stray packaging and module inductances but also due to the actual measurement set-up. Average values of C_{GD} and C_{GS} were taken from the device datasheets since these capacitances are voltage dependent and hence, are not constant during the switching transient. The capacitance used had a fixed value. Attempts to simulate the capacitance were made bud due to the luck of information of the device structure this simulations could not be validated. The values used were based on published work and bibliography. It can be seen in Figure 2.8-3 and Figure 2.8-4 that increasing the gate resistance increases the duration of the gate-turn-ON transient and also dampens the oscillations on V_{GS}.

The modelled and measured V_{DS} transient during MOSFET turn-ON for R_G = 22 Ω and 100 Ω are presented in Figure 2.8-5 and Figure 2.8-6.

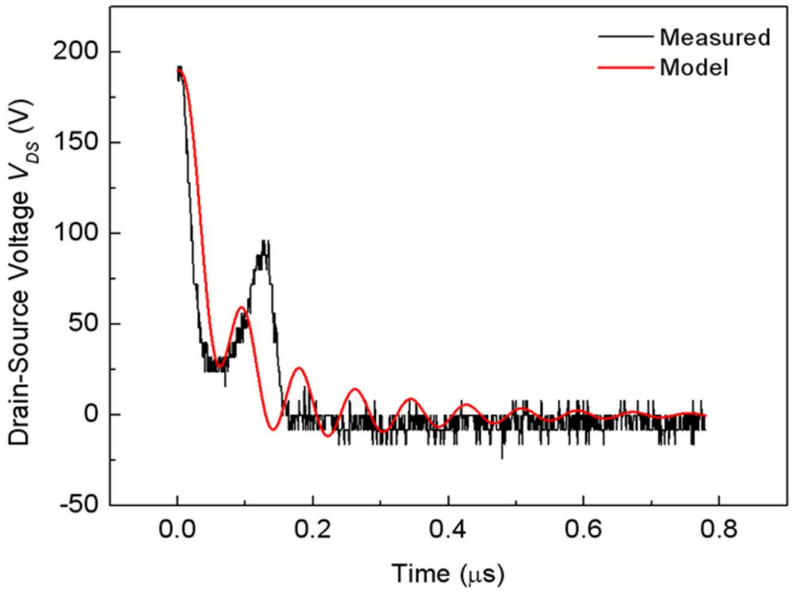


Figure 2.8-5 Experimental and modelled V_{DS} for a gate resistance of 22 Ω

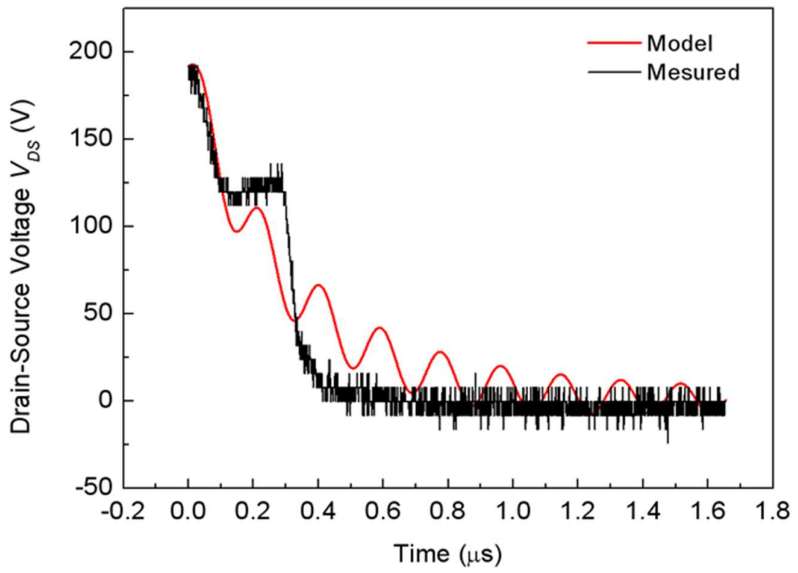


Figure 2.8-6 Experimental and modelled V_{DS} for a gate resistance of 100 Ω

A good correlation between the experimental results and the simulation has been observed for the two gate resistances, with the 100 Ω measurements showing a longer transient. Although the model sufficiently predicts ripples in the V_{DS} turn-ON transient, the variations between the modelled and measured turn on transients are due to the fact that dynamic capacitances are not used in the model. The V_{DS} transient occurs during the discharge of C_{GD}, hence, the model can be further improved if a computationally efficient way of accounting for dynamic capacitances were developed. Figure 2.8-7 shows the impact of the source inductance on the V_{DS} transient. It can be seen that larger source inductances increase the amplitude of the V_{DS} oscillations during turn ON, the graph shows the impact of the source inductance when using a 22Ω resistance. This will also impact the magnitude of the peak voltage over-shoot during turn OFF

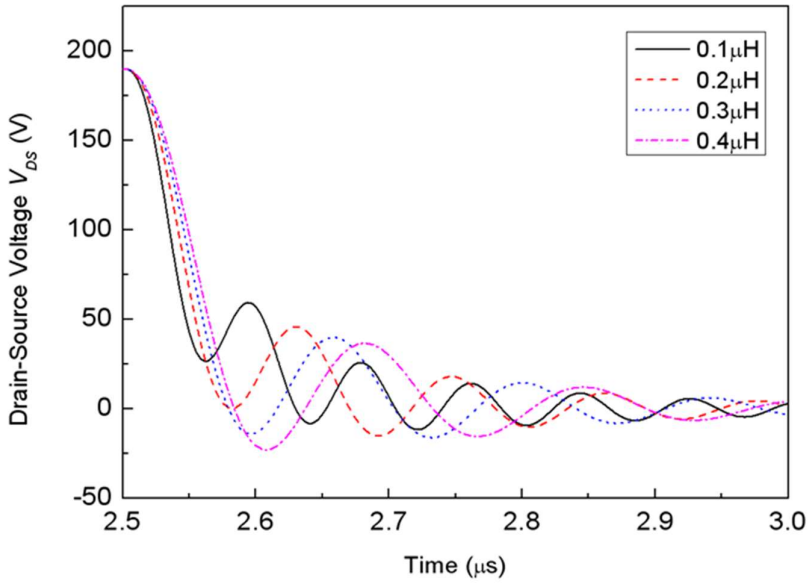


Figure 2.8-7 V_{DS} transient characteristics for different values of L_S

Figure 2.8-8 shows a comparison of the modelled and measured diode voltage (V_{AK}) transients during turn-ON for R_G=22 Ω whereas Figure 2.8-9 shows the diode current (I_{AK}) transients. A good matching is observed in both of them. Figure 2.8-10 and Figure 2.8-11 shows the measured and modelled V_{AK} and I_{AK} transients for R_G=100 Ω where it can be seen that the peak overshoot and the amplitude of the V_{AK} is reduced. The models from $(V_D - V_G)sC_{GD} +$ VD−VDDsLD=0 (2.5-1) to

R

E

F

_

R

e

f

4

4

0

3

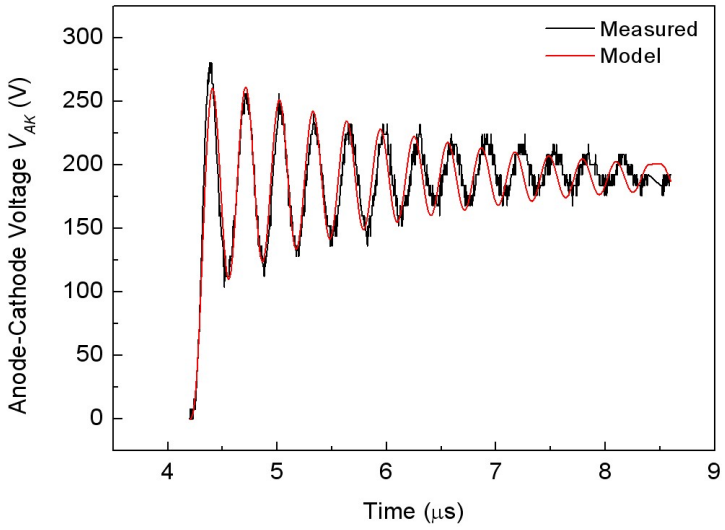


Figure 2.8-8 Experimental and modelled diode transients for a gate resistance of 22 Ω showing V_{AK} vs. time

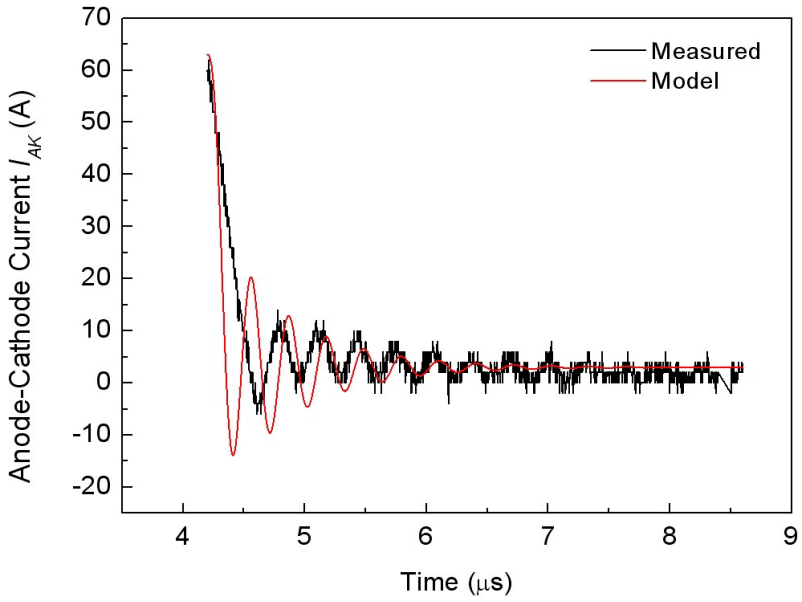


Figure 2.8-9 Experimental and modelled diode transients for a gate resistance of 22 Ω showing I_{AK} vs. time

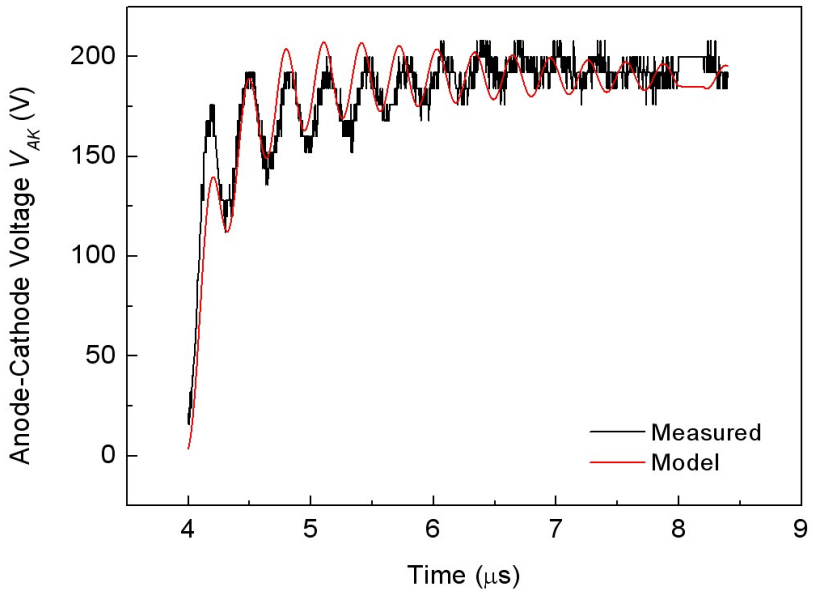


Figure 2.8-10 Experimental and modelled diode transient characteristics for a gate resistance of 100 Ω showing V_{AK} vs. time

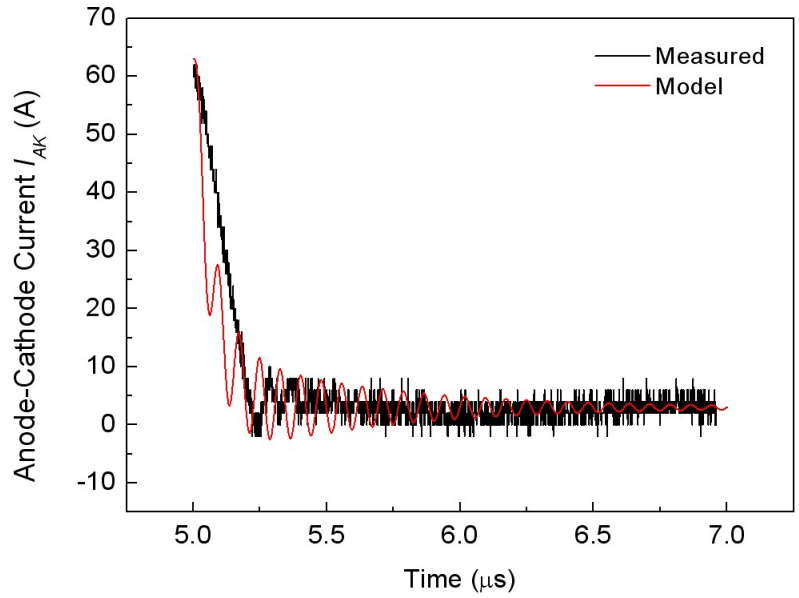


Figure 2.8-11 Experimental and modelled diode transient characteristics for a gate resistance of 100 Ω showing I_{AK} vs. time

2.8.2. Switching Losses

The models developed can be used to estimate the switching losses of hard switched SiC MOSFETs and diodes. In Figure 2.8-12 and Figure 2.8-13 the losses of the MOSFET are presented for both the 22 and 100 Ω gate resistances. It is evident that the power losses are higher for R_G = 100 Ω as expected because of the longer switching duration. The energy

dissipated by the MOSFET when switched with an R_G of 22 Ω is 469.32 mJ for the model and 552.5 mJ for the measurements yielding an error of 15%. For R_G = 100 Ω the model calculates losses of 2457.5 mJ whereas the experimental measurements exhibit 2148.8 mJ yielding an error of 12.56%.

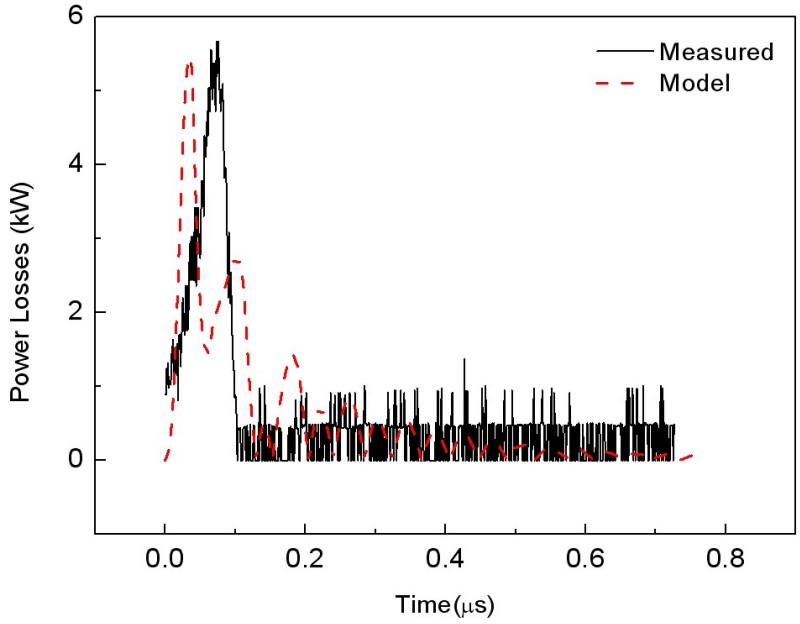


Figure 2.8-12 MOSFET turn on losses for 22Ω gate resistance

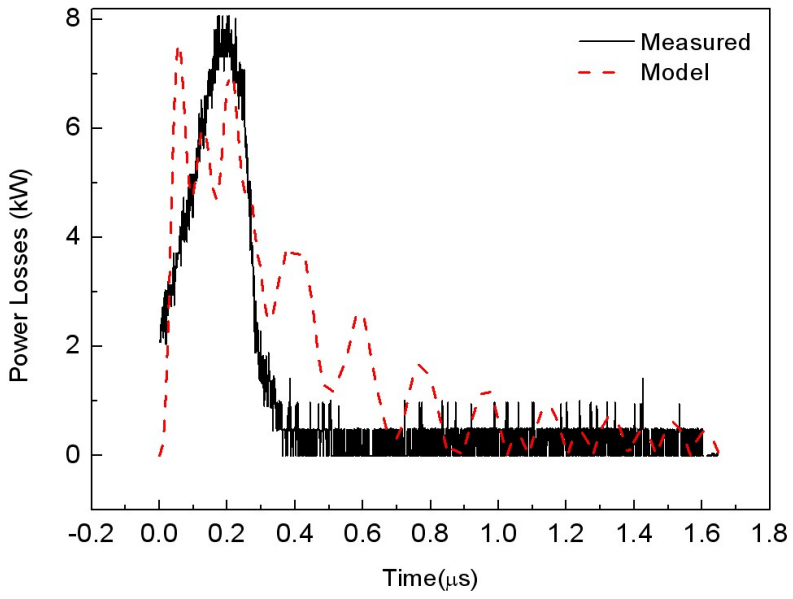


Figure 2.8-13 MOSFET turn on losses for 100Ω gate resistance

The measured and modelled results for the diode losses are presented in Figure 2.8-14 and Figure 2.8-15 for the Figure 2.8-5 and 100 Ω gate resistance switching. Similar to the MOSFET

losses, the diode switching losses increase when R_G goes from 22 Ω to 100 Ω. The losses for the diode when switched with R_G = 22 Ω are 879.3 mJ for the model and 763.1 mJ for the experimental measurements yielding an error of 13%. When switched with RG = 100 Ω, the model calculates 1135 mJ and the measurements exhibit 1063.3 mJ thereby yielding an error of 6.35%. Unlike the MOSFET, the diode shows significant ringing losses in the form of additional power spikes beside the main switching power spike.

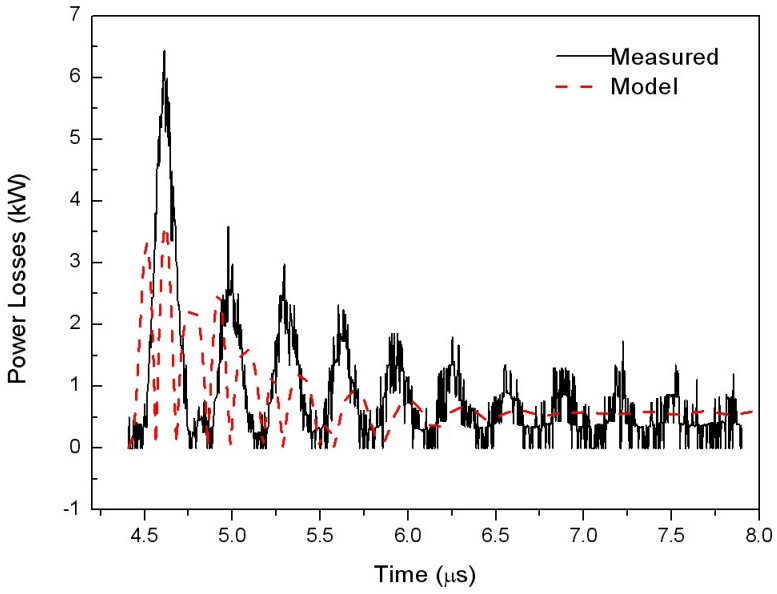


Figure 2.8-14 Diode losses for 22Ω gate resistance

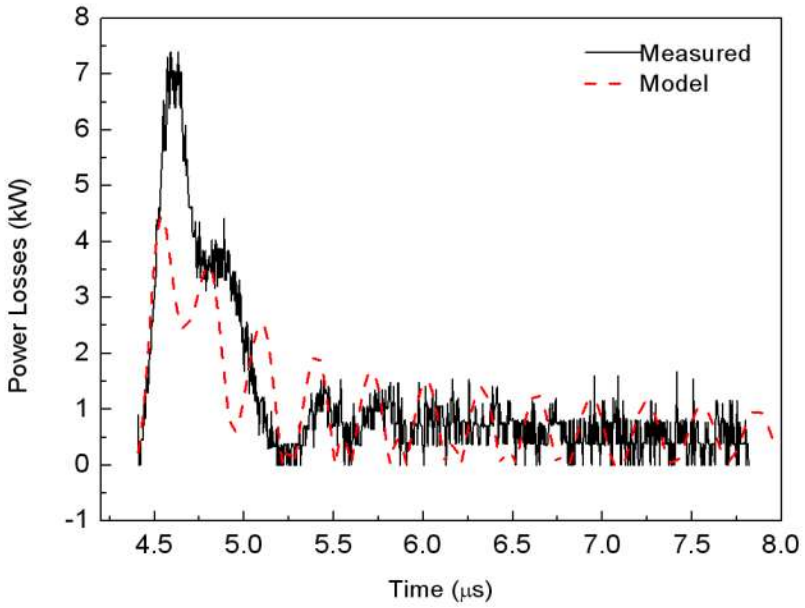


Figure 2.8-15 Diode losses for 100Ω gate resistance

These ringing losses are larger for the device when switched at a 22 Ω gate resistance as a result of the faster switching i.e. larger dI_{DS}/dt. For the MOSFETs, the total measured switching energy losses increases by 74.3% when R_G is increased from 22 Ω to 100 Ω whereas for diodes the loss increases by 28.2%.

2.9. Conclusions

The turn-ON dynamic characteristics of a SiC MOSFET as well as a Schottky SiC diode have been modelled accurately using a new computationally efficient frequency domain technique. The model includes the impact of parasitic inductances. The results show that accounting for parasitic inductances is necessary for correctly simulating the switching and ringing losses. Increasing the gate resistance reduces the ringing losses although at the expense of increasing the switching losses which increase with the gate resistance due to longer transients. Adding a dynamic aspect to the values of the stray capacitors will make the model more precise making the fitting even better. This modelling technique can be used to improve module and packaging design because it enables an accurate assessment of the impact of parasitic inductances.

3. Thyristor Latch-up Mechanisms in Silicon IGBTs

3.1. Forward Blocking Mode in Silicon IGBTs

Like in MOSFETs, BJT, Thyristors and all other power semiconductor devices, the voltage blocking capability of the IGBT is a function of the thickness and the doping of the epitaxial drift layer. The higher the thickness and the resistivity of this layer, the higher the voltage blocking capability. However, excessively thick voltage blocking drift layers will cause unacceptable conduction losses in the forward conduction state. At very high voltages (> 1kV), silicon MOSFETs exhibit unacceptably high conduction losses because of the thickness and resistivity of the voltage blocking layer required to block the OFF-state voltage. Bipolar devices like IGBTs, PiN diodes, Thyristors and BJTs use conductivity modulation to circumvent the problems of high conduction losses faced by unipolar devices. Conductivity modulation occurs when electrons and holes are injected into a low doped voltage blocking drift region to form a high current density plasma that makes on the on-state voltage less dependent on the resistivity of the drift layer. This is why bipolar devices that use conductivity modulation are capable of blocking voltages as high as 6.5 kV whereas unipolar devices are limited to less than 1 kV with the exception of SiC MOSFETs and Schottky diodes. The silicon IGBT is very similar to the silicon MOSFET except for the fact that it is fabricated on a highly doped p-type substrate referred to as the collector. The IGBT is a 4-layer, self-turn-off, voltage controlled, bipolar, power device that comprises of three internal PN junctions. It is a self-turn-off device because, unlike the thyristor, current flow can be interrupted by removing the gate

bias, hence, in this respect, it is similar to a MOSFET. Like the thyristor and BJT, the IGBT is a bipolar device because current flow is due to the drift and diffusion of both electrons and holes, hence, minority carrier lifetime control is key to switching dynamics. Unlike the BJT, the IGBT is voltage controlled because it has a metal-oxide-semiconductor (MOS) interface as the gate structure.

Figure 3.1-1 shows the layer structure of a silicon IGBT under forward mode blocking conditions. This particular structure is that of a non-punch-through (NPT) IGBT. The definition of this will follow in the subsequent section of this chapter. Under forward blocking mode, there is a high positive voltage on the collector of the IGBT while the emitter is at ground (if it is a low side device) or is floating (if it is a high side device). Forward blocking mode is the typical operational mode of IGBTs in voltage source converters with a constant DC link on the DC side. Since the DC link voltage is constant and unchanging, unlike in line commutated current source converters, then the IGBTs in these applications are required to block only in the forward mode. However, in some AC controller applications where the IGBT is connected in the common gate configuration, then bi-directional voltage blocking capability (blocking in both forward and reverse mode) is necessary, however, these applications are a lot less common than voltage source converter applications where basic voltage inversion and rectification is required.

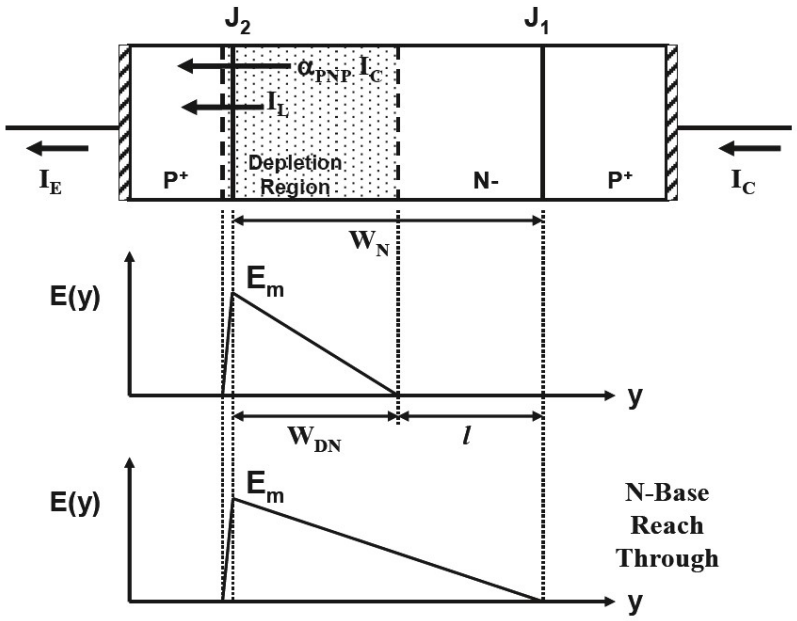


Figure 3.1-1 IGBT in forward blocking mode

With respect to Figure 3.1-1, the IGBT blocks in reverse mode with the voltage on the collector is more negative than the voltage at the emitter. Under forward mode blocking, junction J_2 is the voltage blocking junction that goes into reverse bias. Under reverse blocking mode, junction J_1 is the voltage blocking junction that goes into reverse bias. NPT IGBTs are referred to as symmetrical IGBTs because their forward and reverse blocking characteristics are the same whereas punch-through (PT) IGBTs are referred to as asymmetrical IGBTs because the forward and reverse blocking characteristics are different.

Under forward blocking mode in IGBTs, junction J_1 is forward biased while junction J_2 is reverse biased. This means that there is forward hole injection from the P+ collector into the N-drift region across the forward biased junction. The operational breakdown voltage of the IGBT under forward mode is governed by the open-base BJT breakdown condition. The layer structure in Figure 3.1-1 is identical to that of a PNP BJT with an open N-type base. The current flowing through the PNP structure is a combination of the leakage current comprised of carriers generated within the depletion region of the reverse biased PN junction J_2, and the

collector current comprising of holes injected into N-drift layer from the P+ collector. The total leakage current through the open base PNP BJT can thus be written as:

$$I_C = \alpha_{PNP} I_C + I_L = I_E \qquad (3.1\text{-}1)$$

It should be noted that the injected hole current from the P+ collector is multiplied by the gain of the PNP BJT which is given by α_{NPN}. Hence, the collector current under forward blocking mode in the IGBT can be expressed as:

$$I_C = \frac{I_L}{1-\alpha_{PNP}} \qquad (3.1\text{-}2)$$

From the equation written above, it can be concluded that the IGBT will undergo breakdown in the forward blocking mode when the gain of the open base PNP BJT tends to 1. This open-base gain is dependent on the emitter injection efficiency, the base transport factor and the avalanche multiplication factor.

The emitter injection efficiency is the ratio of injected carriers from the P+ collector into the N- drift region to the total carriers injected on both sides of the PN junction. When a PN junction is under forward bias, there are electrons injected from the N side into the P side and holes are injected in the opposite direction. Because the P+ collector is more heavily doped than the N-drift in NPT (symmetric) IGBTs, the emitter injection efficiency is close to 1.

The base transport factor is a measure of how many injected holes from the forward biased PN junction of the emitter diffuses across the base into the reverse biased base-collector PN junction. It should always be taken into account that the PNP BJT referred to here is the BJT within the IGBT hence the emitter of the BJT is the collector of the IGBT and the collector of the BJT is the p-base of the IGBT. The base transport factor is a function of hole carrier lifetime in the drift region since it will increase with increased lifetime i.e. the higher the hole recombination rate in the N-drift region, the smaller the density of holes that reach the P+ body. The maximum value that the base transport factor can attain in the open base configuration is 1. The base transport factor will increase at higher collector voltages since the depletion width across the N-drift layer increases with the collector bias. The base transport factor is given by:

$$\alpha_T = \frac{1}{\cosh(l/L_p)} \quad (3.1\text{-}3)$$

where l is the length of the un-depleted portion of the total N- drift layer and L_p is the diffusion length of holes in the drift layer. The equation above results from the solution to the diffusion equation of holes in the N-type drift layer. The diffusion of holes in the N-type drift layer is given by the standard diffusion equation below

$$\frac{d^2p}{dy^2} - \frac{p}{L_p^2} = 0 \quad (3.1\text{-}4)$$

The solution to this general equation is given by

$$p(y) = Ae^{-\frac{y}{L_p}} + Be^{\frac{y}{L_p}} \quad (3.1\text{-}5)$$

The distance variable y is taken as the diffusion distance into N drift layer using the P+ collector to N- drift base forward biased PN junction as the zero point. The constants A and B above, depend on the boundary conditions. The boundary conditions are defined at the IGBT collector to base forward biased PN junction and the IGBT base to p-body reverse biased PN junction. The hole concentration at the forward biased P+ collector/N- drift junction is given by

$$p(0) = p_B e^{\frac{qV_{BE}}{kT}} \quad (3.1\text{-}6)$$

In equation (3.1-7) above, V_{BE} is the IGBT collector to base PN junction voltage. The other boundary condition defines the concentration of holes in the N-drift/P-body PN junction which is taken to be zero. The base transport factor is simply the ratio of hole current density at the base-collector junction to the hole current density at the base emitter junction of the PNP BJT within the silicon IGBT.

$$\alpha_T = \frac{J_{pC}}{J_{pE}} = \frac{1}{cosh\left(\frac{W_B}{L_p}\right)} \quad (3.1\text{-}7)$$

The base transport factor increases with the collector voltage because the length of the un-depleted bas region reduces as the collector voltage increases.

The last component in the open-base gain of the IGBT is the avalanche multiplication factor which accounts for the additional carriers generated by impact ionization in the emitter region of the PNP BJT within the IGBT. Electron-hole pairs are generated as the reverse bias electric field sweeps holes across from the N- drift layer into the P+ body of the IGBT. Again, this multiplication factor increases with the collector voltage in a similar manner to the base transport factor.

3.2. Types of IGBTs based on voltage blocking

IGBTs can be categorized based on the type of blocking capabilities. This distinction is based on the internal structure of the device. The major types are the non-punch-through (NPT) IGBTs that have symmetrical blocking capabilities and punch-through (PT) IGBTs that have asymmetrical voltage blocking capabilities. The differences in the doping structures are shown in Figure 3.2-1. In main difference between the NPT and the PT IGBT is the existence of an intermediate highly doped N+ buffer layer between the P+ collector and the low doped voltage blocking N- drift layer in the PT IGBT. In IGBTs, the voltage blocking capability is set by the thickness and the doping of the N- voltage blocking drift layer. Hence, the thickness of this layer is increased with the voltage rating of the IGBT since this layer must support the electric field across the device at its maximum voltage. The breakdown of the P+/N- drift PN junction in the IGBT will be set by two limiting factors. The first factor dictates that the depletion width (space charge region) formed by the reverse bias junction extends across the entirety of the epitaxial layer and reaches through to the p+ collector. This mechanism is called “reach-through” and is not a recommended mode of operation. The second factor is that the maximum electric field formed at the reverse biased PN junction exceeds the critical field of the semiconductor thereby inducing avalanche mode conduction via impact ionization.

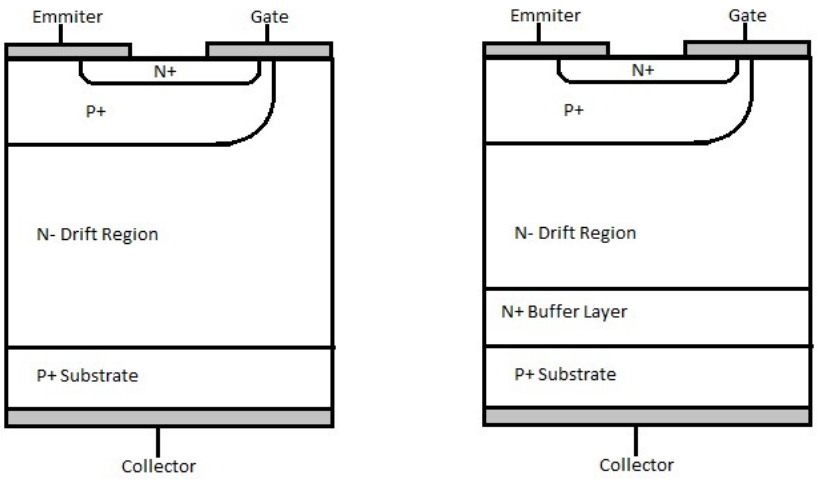


Figure 3.2-1 Non-punch through and punch through IGBT

When the critical field is exceeded, the drift velocity of the carriers generated within the depletion region increases to the point that it can impart sufficient kinetic energy into atoms capable of liberating electron-hole pairs. The critical field of the semiconductor is directly related to the bandgap of the semiconductor since the minimum energy required for electron-hole pair generation is the bandgap. Hence, SiC will have a higher critical field than silicon since it has a wider bandgap than silicon. IGBTs are normally designed to have N- drift layer thicknesses that are sufficiently thick to support the full blocking voltage without exceeding the critical field. Since the N-drift layer is uniformly doped, the spatial gradient of the electric field is linear over the depletion region.

In NPT IGBTs, the profile of the depletion region formed by the blocking voltage is triangular and the maximum voltage blocking capability is set by the reach-through criterion of the maximum depletion width not exceeding the thickness of the N- drift layer. In PT-IGBTs, the presence of the N+ buffer layer between the drift layer and the P+ collector means that there are two distinct spatial gradients of the electric field in the drift layer. One in the low doped N- region and one in the N+ buffer layer. This means that the shape of the electric field in the drift layer is trapezoidal instead of triangular as is the case in NPT IGBTs. Figure 3.2-2 shows the 2D electric field profiles of NPT and PT IGBTs.

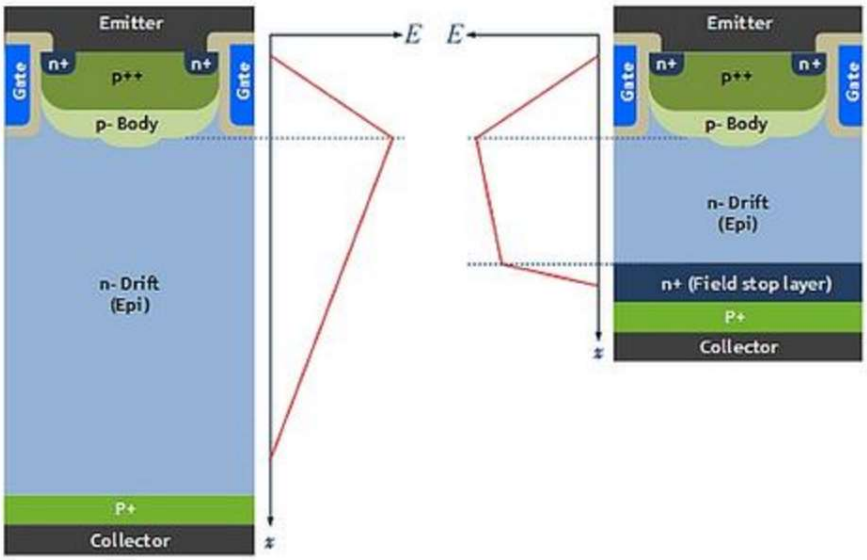


Figure 3.2-2 NPT and PT IGBT Electric Field

Because the rate of depletion width extension over distance is much lower in highly doped layers, PT IGBTs are able to block higher voltages for the same thickness of the N-buffer layer as NPT IGBTs i.e. the area of the trapezoidal electric field profile in the PT-IGBTs is higher than the area of the triangular electric field profile in NPT IGBTs. Hence, this N+ buffer layer is able to improve the conduction of the PT-IGBT compared to the NPT IGBT. Furthermore, during turn-OFF, when minority carrier recombination is required to remove the excess charge stored in the N- drift buffer layer, the performance of the PT-IGBT results in reduced switching losses. This is because minority hole carrier lifetime in the N+ buffer layer is smaller than in the N- drift layer, hence there is a higher recombination rate in the PT-IGBT compared to the NPT IGBT. Hence, the turn-OFF current of an NPT IGBT usually exhibits the long current tail associated with minority carrier recombination during turn-OFF whereas that of a PT-IGBT does not. There are two significant disadvantages of the PT-IGBT compared to the NPT-IGBT and they both relate to reliability. Firstly, PT-IGBTs are capable of exhibiting excessively snappy tail currents due to high carrier recombination rates in the highly doped N+ buffer layer. These high recombination currents result in high turn-OFF dI/dts which when coupled with parasitic emitter/collector inductance from the IGBT packaging may result in excessive voltage

overshoots in the characteristics of the IGBT collector voltage. Secondly, the presence of the N+ buffer layer may lead to a lower temperature coefficient in the ON-state collector to emitter voltage drop at high currents. A positive temperature coefficient, as is the case with NPT IGBTs, guarantees electrothermal stability for parallel connected IGBTs since the hotter device will always conduct less current. However, a negative temperature coefficient in the ON-state voltage may lead to electrothermal instability and current imbalance between the parallel connected IGBTs since the hotter device becomes more conductive.

3.3. Parasitic Thyristor Structure within the IGBT

The power MOSFET has within it, a body diode and a parasitic NPN BJT by virtue of its internal architecture. Likewise, a parasitic IGBT, by virtue of the internal architecture, has a parasitic thyristor since it is a 4 layer device. Figure 3.3-1 shows the vertical cross-section of a silicon IGBT including the N+ emitter, P+ body (for threshold voltage setting), the N- drift (for forward and reverse voltage blocking) and the P+ collector for hole injection in the forward conduction mode. The 3 internal PN junctions in the IGBT are (i) the n-emitter/p-body junction (ii) the p-body/N-drift junction and (iii) the N drift/P collector junction. The presence of these 3 junctions causes two parasitic BJT transistors. One parasitic BJT transistor is an NPN transistor formed between the N+ emitter, P+ body and N-drift while the other parasitic BJT is a PNP transistor formed between the P-body, N-drift and P-collector. As shown in Figure 3.3-2, the collector of the NPN BJT is connected to the base of the PNP BJT (and vice versa), hence a parasitic thyristor is formed. Under normal circumstances, the P+ body of the IGBT should be connected with the N+ emitter, hence, the NPN BJT should not be activated since the base is shorted to the emitter. However, the parasitic p-body resistance, especially when there is lateral current flow, can cause a junction voltage. This is even more so the case at high temperatures when this P-body resistance increases with temperature.

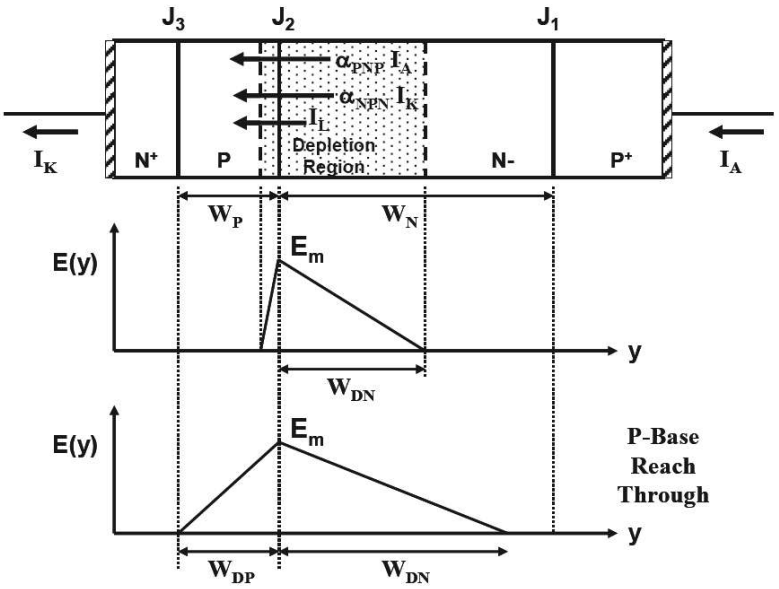


Figure 3.3-1 Vertical Section of IGBT

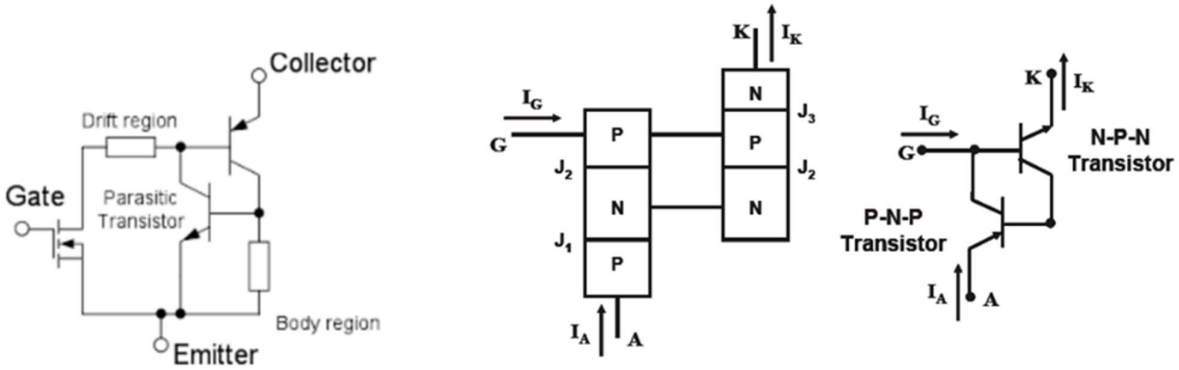


Figure 3.3-2 Parasitic elements in IGBT-equivalent circuits

This parasitic thyristor is not controlled by the gate of the IGBT, hence, when it is activated, it is referred to as “latching”. The latching of this parasitic thyristor is highly undesirable since it can have electrothermally destructive consequences if the latching period is long enough for the junction temperature to rise beyond the device/package limits. As is the case with the classical thyristor, the parasitic thyristor latches when the regenerative current loop between the cross-coupled parasitic BJTs becomes self-sustaining. Assuming that the IGBT is in the forward blocking mode, as shown in Figure 3.3-1, the P+ collector/N-drift junction (J1) and the N+ emitter/P-body junction (J3) is forward biased while the P-body/N-drift junction (J2) is reverse biased. The bulk of the forward voltage is blocked by junction J2

as the depletion width extends through the low doped voltage blocking N-drift layer. Under these conditions, the cathode current is comprised of the leakage current due to carrier generation within the depletion region (I_L), the anode current amplified by the gain of the PNP BJT ($\alpha_{PNP} I_A$) and the cathode current amplified by the gain of the NPN BJT ($\alpha_{PNP} I_A$).

$$I_A = \alpha_{NPN} I_K + \alpha_{PNP} I_A + I_L = I_K \quad (3.3\text{-}1)$$

The gains of the BJTs (α_{NPN}&α_{PNP}) are functions of emitter injection efficiency, base transport factor and the multiplication factor due to impact ionisation. During IGBT turn-OFF, as the collector voltage rises, the expanding depletion width in junction J_2 increases the gain of the parasitic PNP BJT (by increasing the base transport factor) thereby increasing the likelihood of parasitic thyristor latching. The multiplication factor due to impact ionisation also increases with the collector voltage. It is clear from $IA= \alpha_{NPN} I_K + \alpha_{PNP} I_A + I_L = I_K$ (3.3-1) above, that the thyristor within the IGBT latches when the sum of the current gains of the NPN and PNP parasitic BJTs apprach unity.

$$I_A = \frac{I_L}{1-\alpha_{NPN}-\alpha_{PNP}} \quad (3.3\text{-}2)$$

$$\alpha_{NPN} + \alpha_{PNP} = 1 \quad (3.3\text{-}3)$$

There are two modes of latching that can occur in an IGBT namely, (i) static latching which can occur when the device is in forward conduction mode and (ii) dynamic latching which can occur during switching transients.

Dynamic latching occurs when both the collector current and the collector voltage are high. This is something that can occur during switching transients. As it commonly known when we apply a gate emitter voltage on an AC circuit while the device is on the positive side of the collector emitter voltage turns on the device. We can switch off the device with two ways. Either remove the gate emitter voltage or when the device goes into the negative cycle of the AC circuit the device will go into reverse recovery. In this case the dynamic latching current

density is equal with the static latching current density. If we remove the gate emitter voltage the dynamic latching current density will be larger compared to the static.

Static latching happens when the device current density exceeds a certain value. At this state the collector voltage is low but the collector current is high. The latching is not confined into a certain area of the device but it spreads in all of the active area of the device. During static latch up the upper NPN transistor is not inactive anymore and a hole current is going through the P region of the device. This current forward biases the N+ emitter/P-base junction. This hole over plus is creates all over the P base of the device to calculate the voltage drop across the N-P junction a current moving under the length L_E of the emitter can be used. If the resistance of the P base is R_P then

$$V_X = R_P I_\rho \quad (3.3\text{-}4)$$

The hole current is related to the electron current according to:

$$I_p = \frac{\alpha_{PNP} I_n}{(1-\alpha_{PNP})} \quad (3.3\text{-}5)$$

Where α_{PNP} is the gain of the PNP transistor. The emitter current is given from:

$$I_E = I_p + I_n = \frac{I_n}{(1-\alpha_{PNP})} \quad (3.3\text{-}6)$$

Because

$$V_X = \alpha_{PNP} R_P I_{CE} \quad (3.3\text{-}7)$$

And

$$\alpha_{NPN} + \alpha_{PNP} = 1 \quad (3.3\text{-}8)$$

The latching current of the device is described from:

$$I_{L,SS} = \frac{V_{bi}}{(\alpha_{PNP} R_P)} \quad (3.3\text{-}9)$$

But the resistance is proportional to the sheet resistance $\rho_{s,p}$ of the P base so:

$$I_n \propto \frac{V_{bi}}{(\alpha_{PNP} \rho_P L_E)} \quad (3.3\text{-}10)$$

3.4. Thyristor Latch-up Suppression in IGBTs

For thyristor latch-up to occur, the gains of the parasitic NPN and PNP BJTs within the IGBT must sum to 1. Likewise, the resistance in the p-body of the IGBT must be minimized as much as possible since hole current flow across this resistance triggers in the NPN BJT. The parasitic thyristor in the IGBT can be suppressed by (i) ensuring that the gains of the NPN and PNP IGBTs sum to be less than 1 and (ii) minimizing the total resistance along the path of the hole current flow to ensure the emitter-base junction of the NPN BJT is never forward biased. The obvious way of reducing the conductivity of the P-body region is to increase the doping since the equation for the conductivity will be given by

$$\sigma = \frac{1}{pq\mu_p} = \frac{1}{N_A q \mu_p} \qquad (3.4\text{-}1)$$

And the resistivity of the P+ region is

$$\rho_{P+} = \frac{\sigma_{P+}}{t_x} \qquad (3.4\text{-}2)$$

Where t_x is the thickness of the P+ region. However, the threshold voltage is set by the N_A doping since the surface and the body potential within the MOS channel of the IGBT is proportional to the p-body doping. By using a deep P+ body away from the channel, it is possible to suppress the p-body parasitic resistance without affecting the threshold voltage of the IGBT. An IGBT with a deep p-body implant is shown alongside one without a deep p-body implant. The addition of this deep P implant introduces an extra process step which includes an additional ion implantation step. It should be noted that higher junction temperatures increases the likelihood of parasitic thyristor latching since the conductivity of the P-body will decrease as temperature increases.

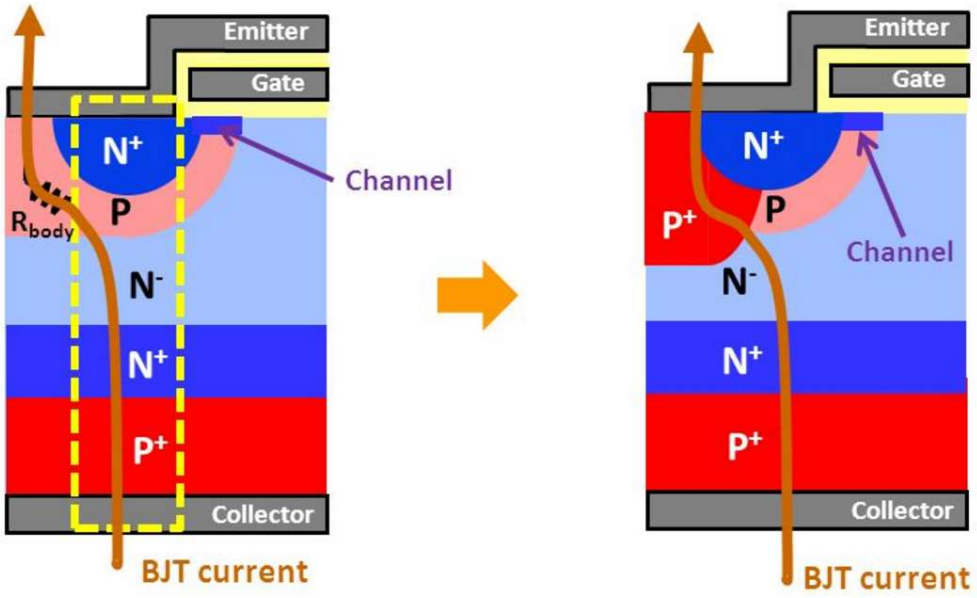


Figure 3.4-1 No P+ body implant compared to a deep P+ body implant

3.5. Hard Commutation with High dV/dt and dI/dt

When silicon IGBTs are used in switch mode, latching of the parasitic thyristor can occur under static and dynamic conditions. Under static conditions, excessively high forward current densities can cause sufficient stray currents (from un-recombined holes diffusing through the IGBT) to forward bias the critical N+ emitter/p-body PN junction. The likelihood of this occurring increases with junction temperature since the parasitic resistance of the IGBT p-body increases with temperature likewise hole minority carrier lifetime. This NPN BJT feeds its collector current into the base of the parasitic PNP BJT in the thyristor. If the sum of the combined gains of both cross-coupled BJTs exceeds unity, and the hole current through the p-body/N-drift junction exceeds the holding current of the parasitic thyristor, then the parasitic thyristor can be activated with potentially destructive electrothermal consequences. Thyristor latching can also occur dynamically during switching through the combination of high turn-off *dI/dt* and parasitic collector inductance causing collector voltage overshoots that exceed the avalanche breakdown voltage rating of the IGBT. In this case, the reverse biased p-body/N-drift junction breaks down and conducts via avalanche mode thereby triggering the parasitic

thyristor. Static thyristor latching is mitigated by sensing and controlling forward currents while dynamic latching is mitigated by IGBT voltage derating and controlled switching sequences. This is not a common failure mode because properly designed and switching IGBTs should avoid this completely.

3.6. Voltage Imbalance in Series Connected IGBTs

Some converter applications require series connection of silicon IGBTs for voltage sharing in the off-state. Voltage imbalance in the off-state can result from variation in leakage currents generated within the voltage blocking depletion regions of the individual IGBTs. Voltage imbalance will occur dynamically if the IGBTs are switched at different rates. Snubbers are used to ensure proper static and dynamic voltage balance in series connected IGBTs, however, in the event of IGBT misfiring, extreme voltage imbalance can occur. In the event of extreme voltage imbalance, avalanche induced thyristor latch-up will occur since the breakdown voltage of the IGBT has been exceeded. In the case of series connected IGBTs where one IGBT is electrothermally destroyed by avalanche induced thyristor latch-up, then failure will occur in a cascaded fashion since the remaining voltage is shared amongst fewer IGBTs. This mode of failure is application related and not device related.

When the IGBT is subjected to an emitter-collector over-voltage surge, either from excessive inductive over-voltage from a poorly designed package with large parasitic inductance or from IGBT misfiring resulting in extreme voltage imbalance in series connected IGBTs, then thyristor latch-up occurs. This happens when the depletion width from the voltage blocking reverse bias junction J_2 reaches the P+ collector/N-drift junction (J1) and punch-through occurs. Here, holes are injected into the N-buffer layer and diffuse through to the p-body where the parasitic NPN transistor is triggered if the combination of the hole current and the parasitic p-body resistance exceeds the PN junction voltage for forward bias. Under these

conditions, the IGBT operates outside its safe operating area with simultaneously higher collector current and voltage. If the inductive overshoot occurs long enough for the heat generated by the thyristor latch-up to cause temperature excursions beyond the device/package limits, then the IGBT is thermally destroyed within a few microseconds. The area of the IGBT with the highest electric field will take all of the current and the resulting failure will create a permanent short within the device. However, if the thyristor latch-up duration is shorter than the time required for IGBT to reach its thermal limits and inductive voltage overshoot is removed sooner, than the IGBT will emerge of avalanching unscathed. There will be no reduced electrothermal or thermo-mechanical reliability.[40-43]

3.7. Experimental Results

As stated the IGBTs can latch up under normal conduction condition as well as when the device is blocking voltage. In applications where a large inductive load is discharged there is a possibility of the IGBT going into avalanche mode conduction. These experiments try to investigate the dependency of ambient temperature as well as calculate the junction temperature of the device under avalanche mode conduction.

The device used for these tests was Fairchild FGA15N120ANTD, it is a 1.2kV 30A Trench IGBT . The experimental set up as well as the circuit diagram is presented Figure 3.7-1

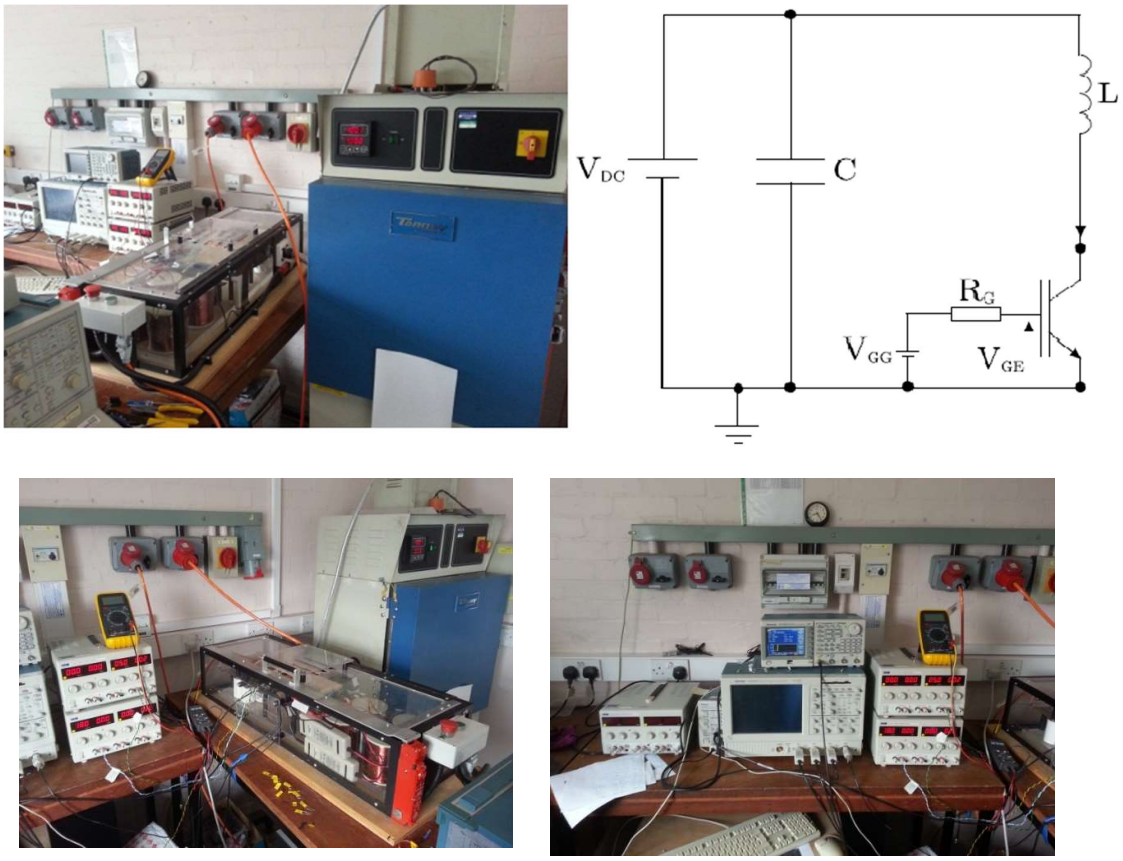


Figure 3.7-1 Experimental set up

The devices were tested in 6 different temperatures inside an environmental chamber. The performance of the device was examined under 35A different avalanche current using an inductor of 1.1mH. The gate resistance used was 56Ω, the value of the resistance is not that vital because the device is undergoing a singular switching event and the time that it takes for their device to turn on is not important for the test. It is necessary to point out that the device was in the environmental chamber for 20 minutes without any voltage applied to it. The reason was so that the junction temperature would be the same as ambient. The drain source voltage, drain source current and gate voltage are presented in the following figures. For each of the tests conducted at different temperatures regardless if the device was destroyed after the test or not a new device was used to avoid pseudo results due to device fatigue. To make sure tthat the devices used was of similar characteristics a large number was ordered from the same

supplier in a single order. This ensures the devices will come from the same wafer so they will have similar characteristics

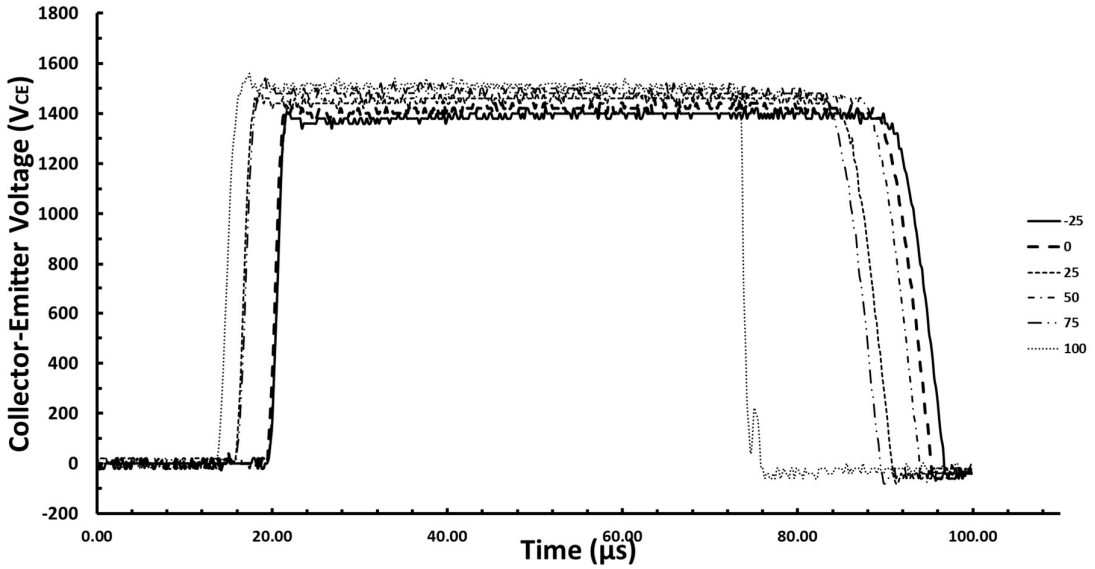


Figure 3.7-2 Collector Emitter Voltage

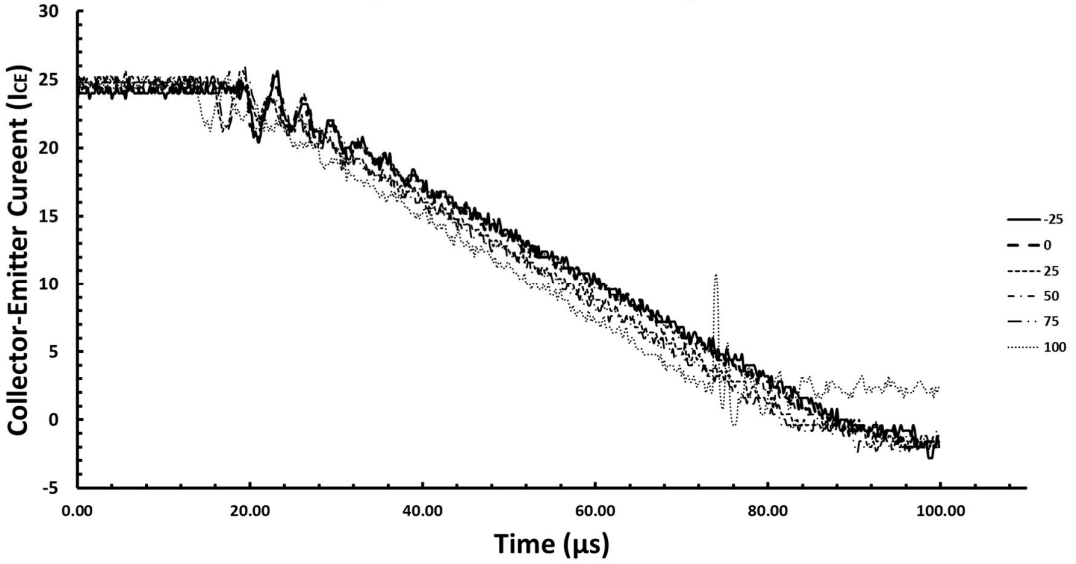


Figure 3.7-3 Collector Emitter Current

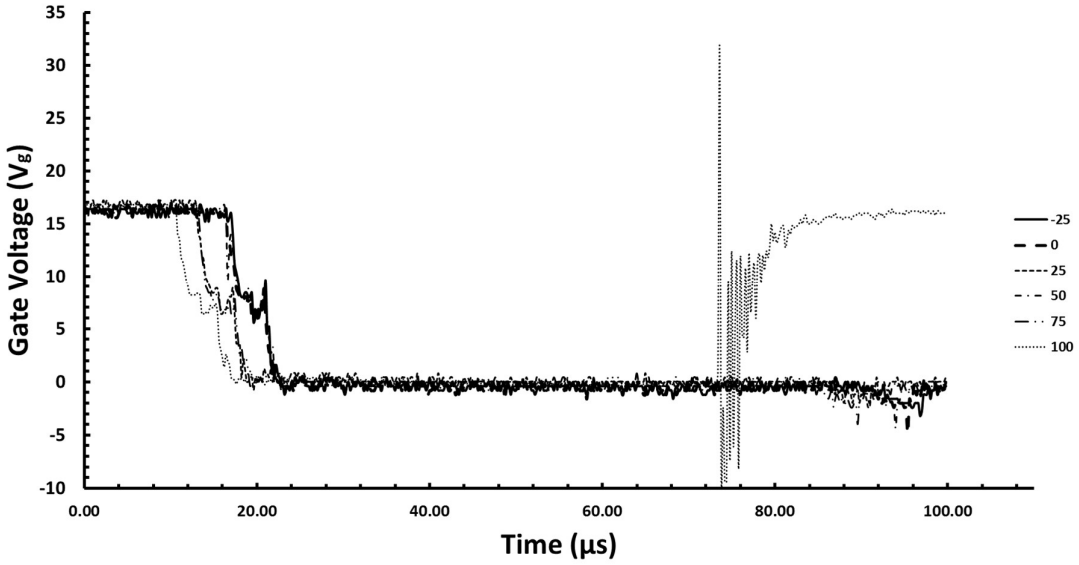


Figure 3.7-4 Gate Voltage

All of the devices were not damaged during avalanche mode conduction except the device that was at 100ºC. This is the reason the gate of this particular device is so abnormal at the turn off as well the current. Also the duration of the switching event is smaller because of the failure of the device. This shows that temperature is a decisive factor if the device is going to go into avalanche. The resistance of the IGBT during avalanche is calculated.

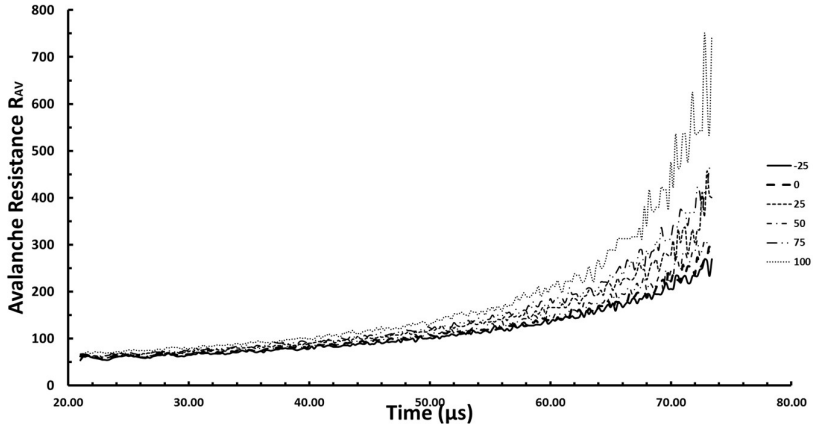


Figure 3.7-5 Avalanche Resistance

It is not very evident form this graph but the resistance is increasing while the temperature is increasing. To make it easier to visualize a curve fitting for all the curves has been performed. These are the equations as well as the figure of the curve fitting

$$R_{-25} = 2.637^{-6}t^{4.197} + 61.84 \qquad (3.7\text{-}1)$$

$$R_0 = 1.101^{-6}t^{4.416} + 64.98 \quad (3.7\text{-}2)$$

$$R_{25} = 1.638^{-8}t^{5.415} + 73.92 \quad (3.7\text{-}3)$$

$$R_{50} = 3.099^{-7}t^{4.741} + 67.17 \quad (3.7\text{-}4)$$

$$R_{75} = 6.971^{-9}t^{5.713} + 76.89 \quad (3.7\text{-}5)$$

$$R_{100} = 1.051^{-11}t^{7.328} + 87.68 \quad (3.7\text{-}6)$$

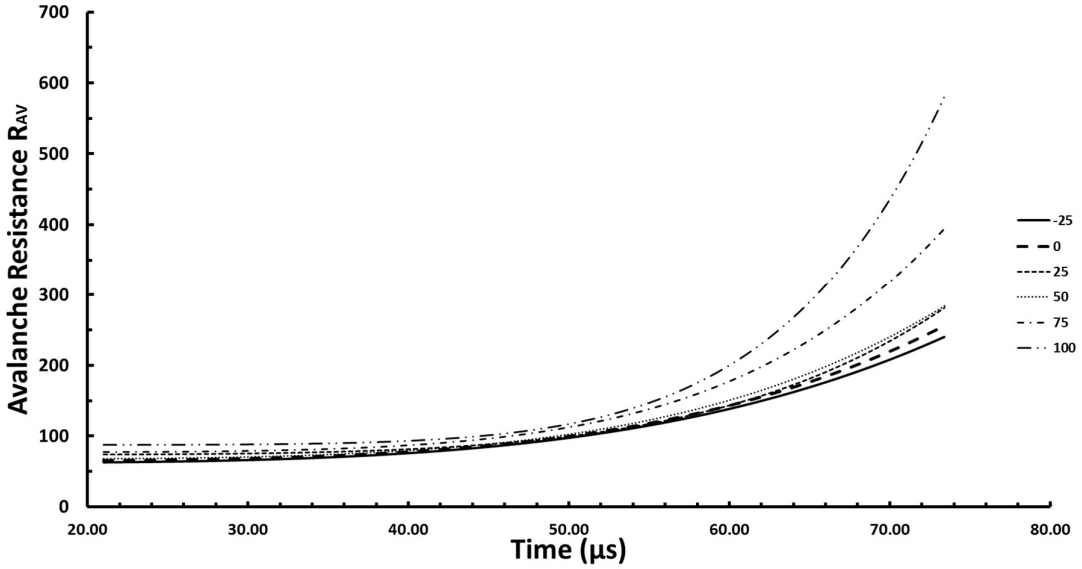


Figure 3.7-6 Avalanche resistance fitting curves

From the curve fitting it is very clear that the resistance of the transistor is increasing with temperature. The increase is not linear so the effect will be even more severe in the device reliability. The resistance is a combination of all the layers of the device and it is determined mostly from the N drift region of the device. Despite that the P+ Region resistance of the device will increase as well making the device more prone to latching up. Keeping the device in low temperatures, in applications that require from the device to go into avalanche is vital for its The mobility of the holes, responsible for the resistivity of the device as shown form equation $\rho P+= \frac{\sigma_{P+}}{t_x}$ (3.4-2) depends on the mobility of the device. The mobility is dependent on temperature. The equation that describes the mobility of holes in respect to temperature is[6]:

$$\mu_P = 495\left(\frac{T}{300}\right)^{-2.2} \quad (3.7\text{-}7)$$

The amount of energy that the power device has to handle is massive. For this reason it is wrong to assume that the temperature of the junction remains stable during avalanche. Because of the small duration of the pulse only the first value of the thermal resistance in the Foster network is important. Also the combination of a small pulse and the small value of the thermal capacitance of the junction allow to ignore the contribution of the thermal capacitance to the system. To calculate the Junction temperature we use

$$T_J = R_{th}Q - T_0 \qquad (3.7\text{-}8)$$

Where T_J is the Junction temperature, R_{th} is the thermal resistance. Q is the heat dissipated and T_o ambient temperature. The thermal resistance of the Junction is very small, 0.0011 ºC/W. This value was calculated from the device datasheet. The results of the junction temperature are presented in the next figure

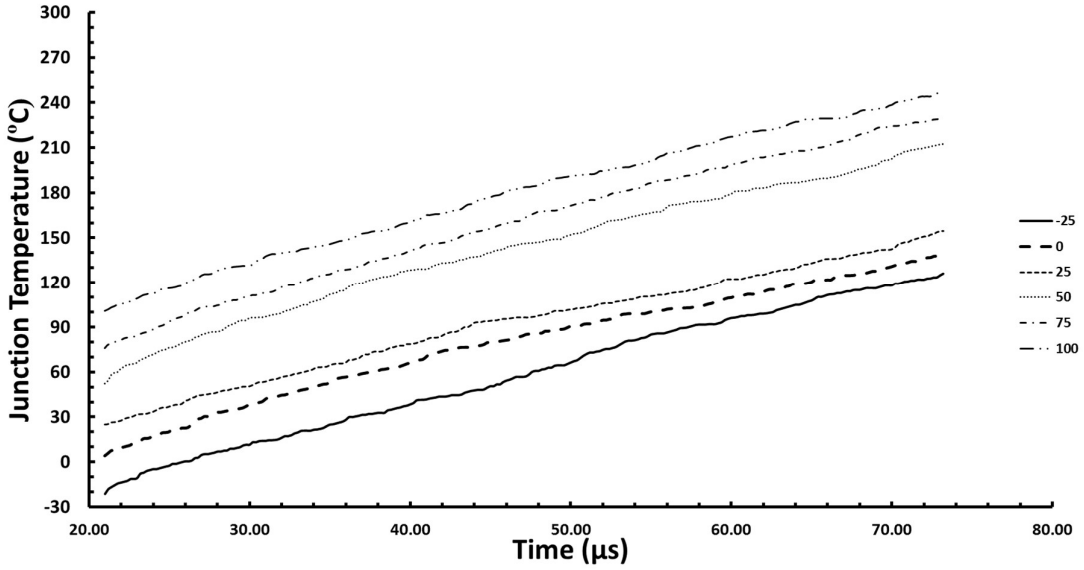


Figure 3.7-7 Junction Temperature

And the mobility results are

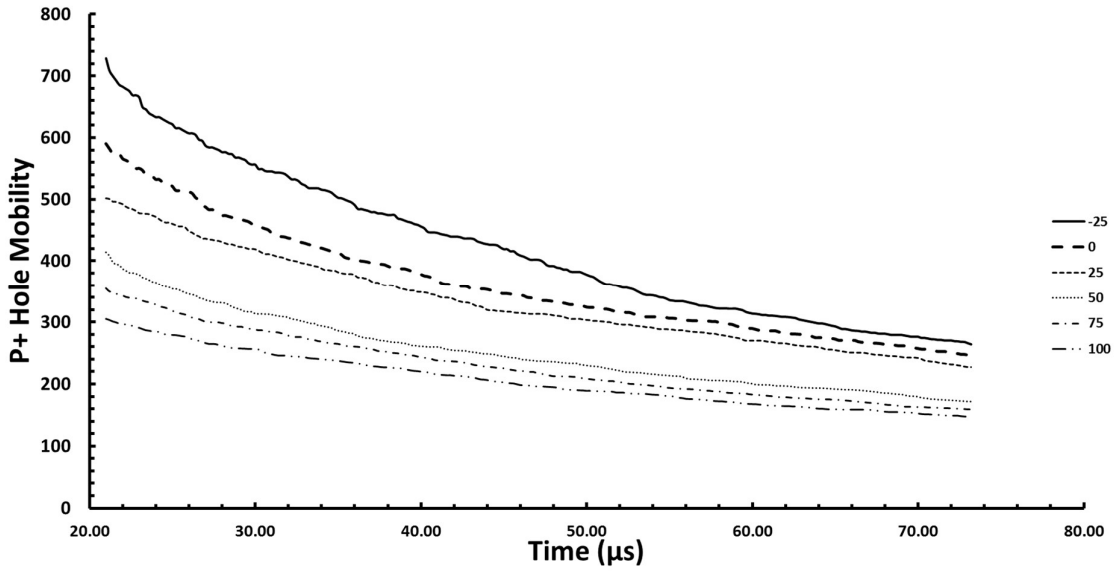


Figure 3.7-8 P+ Region hole mobility

To investigate how the current gain of the PNP transistor is altered it is necessary to have structural information about the device, information that any company is willing to share,

The gain of the transistor is given from

$$\alpha_{PNP} = \frac{1}{\cosh\left({W_D}/{L_A}\right)} \quad (3.7\text{-}9)$$

Where W_D is the base width and L_A is the ambipolar diffusion length

The ambipolar diffusion length is calculated using

$$L_A = \sqrt{D_a \tau_\alpha} \quad (3.7\text{-}10)$$

Where D_a is ambipolar diffusion coefficient and τ_a is the carrier lifetime. Carrier lifetime is affected from temperature but not as much as the diffusion coefficient so it is safe to assume it doesn't play such a significant role [44].

$$D_a = \frac{2D_n D_p}{D_n + D_p} \quad (3.7\text{-}11)$$

Where D_n and D_p are the electron and hole diffusion coefficient. They are calculated using

$$D = \frac{kT}{q}\mu \quad (3.7\text{-}12)$$

The mobility of electrons into Si is

$$\mu_n = 1360\left(\frac{T}{300}\right)^{-2.42} \qquad (3.7\text{-}13)$$

The electron mobility based on the junction temperature is presented in the next figure.

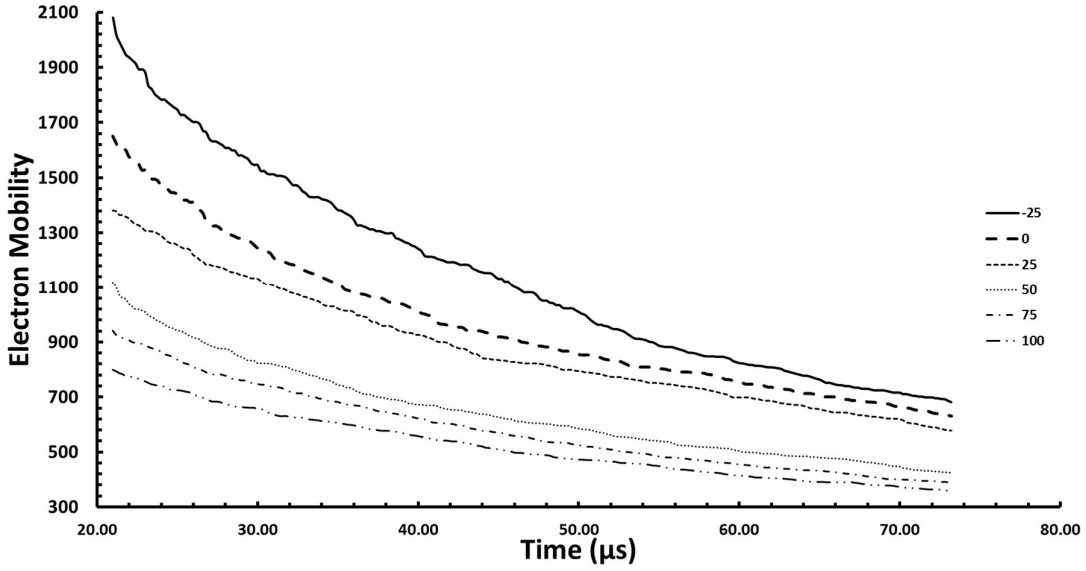


Figure 3.7-9 electron mobility

Due to the nature of the formula for the current gain and because it is dependent from cosh it is impossible to come to conclusions on the value of the current gain without getting the necessary information. In principal cosh is a function that is very monotonous when it approaches zero so any small change around that area will have a significant effect.

4. Improved Electrothermal Ruggedness in SiC MOSFETs Compared with Silicon IGBTs

4.1. Introduction to Avalanche mode conduction and Impact ionization

One of the most important attributes of a power semiconductor device is the ability to block the required voltage of the application it is used in. In a voltage source converter, this is usually the DC link voltage. The semiconductor will have limits on how much voltage it can block. The maximum voltage blocking capability of a power device will be set by the thickness of the voltage blocking layers, the resistivity of the layers and the critical field of the semiconductor material. In MOSFETs, IGBTs and PiN diodes, the voltage blocking action is due to the depletion formed at the reverse biased PN junction. In Schottky diodes, voltage blocking is due to the metal-semiconductor rectifying (or Schottky) contact. Due to high electric fields generated at the edges of device, breakdown usually occurs there, hence, devices are designed with appropriate edge terminations that can support the breakdown voltage. Carriers in the depletion region are accelerated by the high electric fields generated by the blocking voltage. These carriers, which can be either holes or electrons, are produced by diffusion from adjacent quasi-neutral regions or by the space charge generation phenomenon. As the blocking voltage increases, these carriers gain sufficient kinetic energy which, when transferred to the lattice of the semiconductor through collision, is capable of exciting electrons from the valence band to the conduction band i.e. if the energy dissipated by the free carrier into the lattice is greater than the bandgap of the semiconductor, then an electron-hole pair is generated. The process of generating electrons or holes as a result of high electric fields accelerating carriers with sufficient energy is referred as impact ionization. The electron hole pairs created from the impact ionization also under go electric field induced acceleration and repeat the process of

lattice scattering thereby generating more electron-hole pairs similar to a chain-reaction. If this process is self-sustained and sufficient carriers are generated for a current to flow, the device has undergone avalanche breakdown since it can no longer block the voltage. Avalanche breakdown is one of the main reasons devices have a maximum operating voltage. A way of defining how prone a device is to avalanche mode conduction is by determining coefficients that can be calculated or measured. In this case we define the impact ionization coefficient and the avalanche multiplication factor.

The impact ionization coefficient is defined as the number of electron hole pairs that are created by a mobile carrier travelling through 1cm of the depletion region along the direction of the electric field. It is evident that the impact ionization coefficient is strongly dependent from the electric field applied to the device. The values for Si and SiC respectively are:

$$\alpha_F(Si) = 1.8 \times 10^{-35} E^7 \qquad (4.1\text{-}1)$$

$$\alpha_B(4H - SiC) = 3.9 \times 10^{-42} E^7 \qquad (4.1\text{-}2)$$

Device breakdown by avalanche multiplication occurs when the impact ionization coefficient approaches infinity. A mathematical expression for this can be developed by considering a one dimensional reversed biased P-N junction with the depletion region mostly occurring in the P region of the junction. If an electron hole pair is created at a distance x from the junction of the device, the hole will drift towards the negatively biased P terminal of the reverse biased junction while the electron will drift towards the positively biased N terminal of the junction. If the electric field is large enough, these mobile carriers will gain sufficient kinetic energy to generate more electron-hole pairs through the previously described process of impact ionization. Based on the definition of the impact ionization coefficient, the hole will generate a hole-electron pair of $\alpha_P \cdot dx$ travelling through the depletion region. At the same time the electron will generate another pair $\alpha_n \cdot dx$. The total number of electron hole pairs that will created from a single pair of electron hole will be:

$$M(x) = 1 + \int_0^x a_n M(x)dx + \int_x^W a_P M(x)dx \quad (4.1\text{-}3)$$

where W is the width of the depletion layer. A solution to this equation is:

$$M(x) = M(0)exp\left[\int_0^x (a_n - a_P)dx\right] \quad (4.1\text{-}4)$$

Where M(0) is the the total number of electron–hole pairs at the edge of the depletion Region. Using equation $M(x) = 1 + \int_0^x a_n M(x)dx + \int_x^W a_P M(x)dx$ (4.1-3)with x=0.

$$M(0) = \left\{1 - \int_0^W a_P exp\left[\int_0^x (a_n - a_P)dx\right]dx\right\}^{-1} \quad (4.1\text{-}5)$$

Using $M(x) = 1 + \int_0^x a_n M(x)dx + \int_x^W a_P M(x)dx$ (4.1-3) and $Mx=M(0)exp\left[\int_0^x (a_n - a_P)dx\right]$(4.1-4)

$$M(x) = \frac{\exp[\int_0^x (a_n - a_P)]}{\left\{1 - \int_0^W a_P exp\left[\int_0^x (a_n - a_P)dx\right]dx\right\}} \quad (4.1\text{-}6)$$

Equation $M(x) = \frac{\exp[\int_0^x (a_n - a_P)]}{\left\{1 - \int_0^W a_P exp\left[\int_0^x (a_n - a_P)dx\right]dx\right\}}$ (4.1-6) is the multiplication coefficient which allows for the calculation of the number of electron hole pairs that are generated at a certain distance from the junction if we know the distribution of the electric field. The avalanche breakdown condition stated earlier reaching infinity corresponds to M becoming equal to infinity. This requires the denominator of equation $M(x) = \frac{\exp[\int_0^x (a_n - a_P)]}{\left\{1 - \int_0^W a_P exp\left[\int_0^x (a_n - a_P)dx\right]dx\right\}}$ (4.1-6) to become zero [6].

4.2.Avalanche Breakdown in Power Devices

Power devices are usually designed not to operate in avalanche mode conduction although there are some exceptions in low voltage automotive applications. However, there is a requirement to withstand avalanche events that result from the unclamped inductive switching (UIS) of inductive loads like machine coil windings, applications like automotive ABS systems

or injector coils. The breakdown voltage of the device is set according to the limit for avalanche breakdown in the critical junctions of the device.

Power MOSFETs: In power MOSFETs, there is an integral body diode formed between the p-type body and the n- drift layer. This is called the body diode and is a PiN diode because of the low doped n-drift layer between the p-body and the n+ drain. The p+ body is usually shorted directly with the n+ source so as to reduce if not eliminate floating body effects which are core to the mechanism of parasitic BJT latch-up as will be discussed further in this chapter. The breakdown voltage of the MOSFET is set by the maximum reverse bias that this body diode can sustain without avalanche breakdown, although the edge termination also plays a crucial role is setting the breakdown voltage. Severe over-voltages resulting from high current commutation rates in the presence of parasitic inductance can also result in avalanche breakdown and potential catastrophic failure of the MOSFET. The parasitic NPN BJT inherent in power MOSFETs can be a trigger mechanism for the initiation of avalanche breakdown. This will be discussed in further detail for SiC power MOSFETs.

Power Diodes: PiN and Schottky diodes can suffer avalanche breakdown if subjected to voltages beyond the maximum rating. Because diodes are less complex than MOSFETs, there is no parasitic BJT, hence, latch-up is not possible in diodes. Catastrophic failure can occur in diodes if the instantaneous power dissipated within the diode during avalanche breakdown causes the junction temperature to rise beyond the thermal limits of the diode. The semiconductor material from which the diode is fabricated will have a significant impact on its avalanche ruggedness with SiC diodes exhibiting significantly more ruggedness compared with silicon diodes because of the wide bandgap characteristics.

Silicon IGBTs: IGBTs are typically not avalanche rated in the same way MOSFETs are. Unlike MOSFETs that have 3 layers (and 2 PN junctions), IGBTs have 4 layers and have 3 PN junctions. Hence, IGBTs have a parasitic thyristor instead of a parasitic BJT. Instead of an

internal body diode anti-parallel to the IGBT, there is an internal PNP transistor. This PNP transistor will typically be more prone to triggering impact ionization induced avalanche breakdown compared to a parasitic diode. IGBTs are always therefore used with external discrete anti-parallel diodes for reverse conduction and for avalanche conduction as well. The parasitic thyristor is latched in a similar was to a phase controlled thyristor i.e. when there is a positive regenerative avalanche breakdown between the internal PNP transistor and the NPN transistor within the IGBT. The presence of several junctions and stored charge makes IGBTs less avalanche rugged than MOSFETs.

Thyristors: Thyristors operate through latching. The thyristor is a 4 layer PNPN device that can block both forward and reverse voltages. The thyristor is comprised of an NPN and a PNP BJT with the collector of each BJT connected to the base of the other. The thyristor is switched ON or latched when there is a self-sustaining positive regenerative action between the 2 BJTs since an increase in the collector current of one BJT causes an increase in the base current of the other. To initiate this, an initial base current is needed through the gate of the thyristor. The only way to stop current conduction is by anode-to-cathode voltage reversal, which is why thyristors are typically used in line-commutated converters since they lack self-turn-OFF capability. Thyristors, again, are not usually avalanche rated.

4.3. MOSFET Parasitic BJT

Electrothermal ruggedness is an important reliability metric that quantifies the ability of the power semiconductor device to withstand electrothermal stresses. This electrothermal stress can result from the conduction under avalanche mode where there is simultaneously high current flowing through the device and a high voltage across it. Some circuits purposely use MOSFETs in unclamped inductive switching (UIS) mode, but these are mainly automotive applications where the devices drive inductive loads without anti-parallel free-wheeling diodes

to commutate the current when the device is switched off [36, 45-47]. Avalanche mode conduction can also be triggered by high *dV/dt* transients which coupled with parasitic capacitances, can cause a body current to flow thereby forward biasing the emitter-base junction of the parasitic BJT[48]. The body current is usually generated by the charging of a depletion capacitance during voltage switching. MOSFETs can also suffer severe electrothermal stresses in forward mode conduction if biased in the linear mode (high current and high voltage conditions)[49]. It should be noted that linear mode bias refers to the saturation mode bias in MOSFETs ($V_{DS}>V_{GS}-V_{TH}$), however, because the condition was first considered for BJTs, the term linear mode (which for a MOSFET is the ohmic or triode region), has repeatedly been used for MOSFETs as well. Linear mode conduction can also occur during switching transients when the bias point of the device moves across the load line. However, since the electrical switching time constant is much smaller than the thermal time constant, it is less of a problem for reliable switch mode power MOSFETs.

All power MOSFETs, by virtue of their physical design, have anti-parallel diodes as well as parasitic NPN BJTs. In case the voltage applied to the device is larger than the breakdown voltage of the device the P-N junction electric field will reach a point where the avalanche mechanism will commence. Research has shown that the maximum electric field happens in the corner of the P well. Ideally, the p-body of the MOSFET should be shorted to the source either by a high p-body implant dose away from the MOSFET channel (so as not to increase the threshold voltage excessively)[50] or by a moat structure with metal deposition shorting the n-source to the p-body.

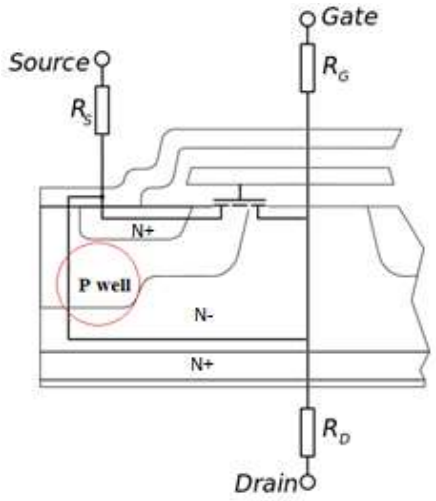


Figure 4.3-1 MOSFET with deeper p-well

The purpose of shorting the body to the source is to ensure that there is no forward voltage drop between the body and the source. In reality, there is always some resistance between the source and the body; and this resistance will increase with temperature. Figure 4.3-2 shows the schematic of a vertical DMOSFET and the corresponding circuit model showing the additional anti-parallel diode and NPN parasitic BJT[51].

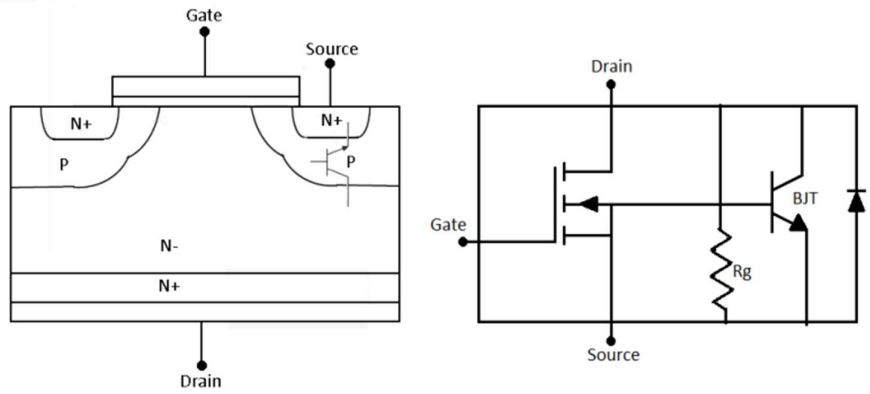


Figure 4.3-2 MOSFET Schematic diagram and equivalent circuit showing the anti-parallel diode and NPN Transistor.

When current is flowing from the drain to the source through the channel, sufficient stray current flowing through the source-to-body resistance can cause the voltage drop across the source-body junction to forward bias the emitter-base junction of the parasitic BJT. Avalanche breakdown may be triggered when the resistance of the P body of the device is big enough to

turn on the parasitic BJT and if the stray body current is high enough to forward bias the P-N junction of the device thereby turning the parasitic bipolar device on. The likelihood of this increases with temperature because of the positive temperature coefficient of the body resistance and the negative temperature coefficient of the in-built voltage across the source-body junction of the MOSFET (emitter-base junction of the parasitic BJT)[52]. Because BJT collector currents have a positive temperature coefficient, they are inherently unstable at high temperatures as a result of thermal runaway i.e. a positive feedback process between current and temperature. In reality, power MOSFETs are comprised of numerous smaller FET cells sharing the same terminals. In ideal conditions these smaller FET cells should share current equally. However, process induced non-uniformities mean that there is always some current mal-distribution. Therefore, process induced electrical and thermal non-uniformities across the MOSFET cells will further enhance thermal runaway through current crowding. To mitigate this, unclamped inductive switching tests are usually done in the production line to screen out defective devices with process induced non-uniformities that may compromise electrothermal ruggedness [48, 53].

The total energy dissipated by the power MOSFET under avalanche mode conduction is determined by the peak magnitude of the avalanche current and the size of the inductor subjecting the device to UIS. During the avalanche event, the current linearly decreases to zero at the rate that is inversely proportional to the inductance. The peak magnitude of the current will depend on the initial current flowing through the transistor. A typical test circuit is shown in Figure 4.3-3 below, where the power supply, the MOSFET to be subjected to avalanche (DUT) and the inductor are shown.

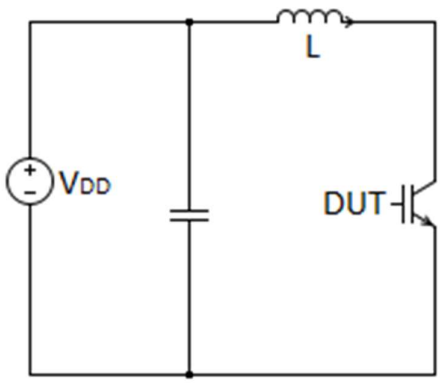


Figure 4.3-3 Avalanche UIS test circuit

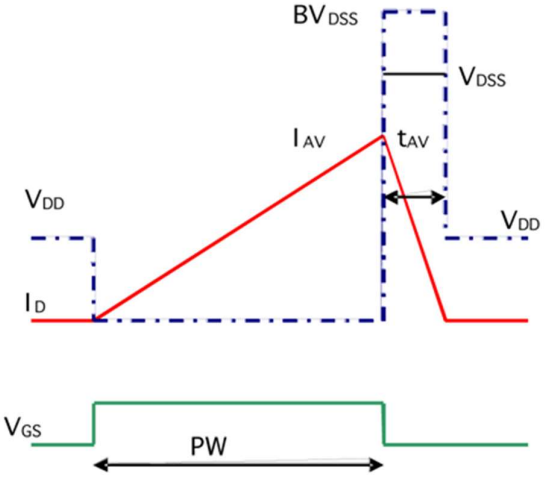


Figure 4.3-4 Device under avalanche[54]

Considering that the DUT is initially conducting and the inductor is charging, applying KVL to the circuit yields the equation below

$$V = L\frac{dI}{dt} + V_{DD} \qquad (4.3\text{-}1)$$

When the DUT is turned OFF, the KVL equation for the circuit becomes

$$L\frac{dI}{dt} = V_{BR} - V_{DD} \qquad (4.3\text{-}2)$$

Assuming a constant rate of change of current, the current through the DUT during avalanche can be expressed as

$$I = \left(\frac{V_{BR}-V_{DD}}{L}\right)t \qquad (4.3\text{-}3)$$

Where *t* is the avalanche duration.

Since, the voltage across the device during avalanche is the breakdown voltage of the DUT, then, the total power dissipated by the DUT is given by

$$P = IV = V_{BR}\left(\frac{V_{BR}-V_{DD}}{L}\right)t \quad (4.3\text{-}4)$$

The energy is the integration of the avalanche power over time

$$E = \int_0^t V_{BR}\left(\frac{V_{BR}-V_{DD}}{L}\right)t\,.\,dt = \frac{V_{BR}}{2}\left(\frac{V_{BR}-V_{DD}}{L}\right)t^2 \quad (4.3\text{-}5)$$

Since the avalanche duration is given by $t = L\frac{I}{(V_{BR}-V_{DD})}$, then the total avalanche energy dissipated by the DUT can be written as

$$E = \frac{1}{2}{I_o}^2 L\left[\frac{V_{BR}}{V_{BR}-V_{DD}}\right] \quad (4.3\text{-}6)$$

Due to the fact that there is simultaneously high voltage across the device as the avalanche current flows through it, hence, there is high instantaneous power dissipation. It is vital then to be able to calculate the maximum temperature rise of the device:

$$\Delta T_M = \frac{\sqrt{2}}{3}P_o K\sqrt{t_{AV}} \quad (4.3\text{-}7)$$

Where $K = \frac{2}{A\sqrt{(\rho\pi kc)}} = 2\sqrt{\frac{R}{\pi C}}$ (4.3-8)

ΔT_M is the temperature rise of the device, A The chip area, ρ the density of the material, k the thermal conductivity of the device, c the specific heat of the material, R the thermal resistance

$$\Delta T_M = \frac{\sqrt{2}}{3}P_o K\sqrt{\frac{LI_o}{V_{BR}}} \quad (4.3\text{-}9)$$

4.4. Experimental Measurements

A 1.2 kV/24 A SiC MOSFET and a 1.2 kV/30 A silicon IGBT have been tested in unclamped inductive switching circuits at different temperatures. The devices have been tested to destruction at different ambient temperatures

4.4.1. Avalanche Performance at several temperatures

Figure 4.4-1 shows the experimental set-up and the circuit diagram which includes a gate-drive circuit, the environmental chamber, test enclosure, power supplies and oscilloscopes.

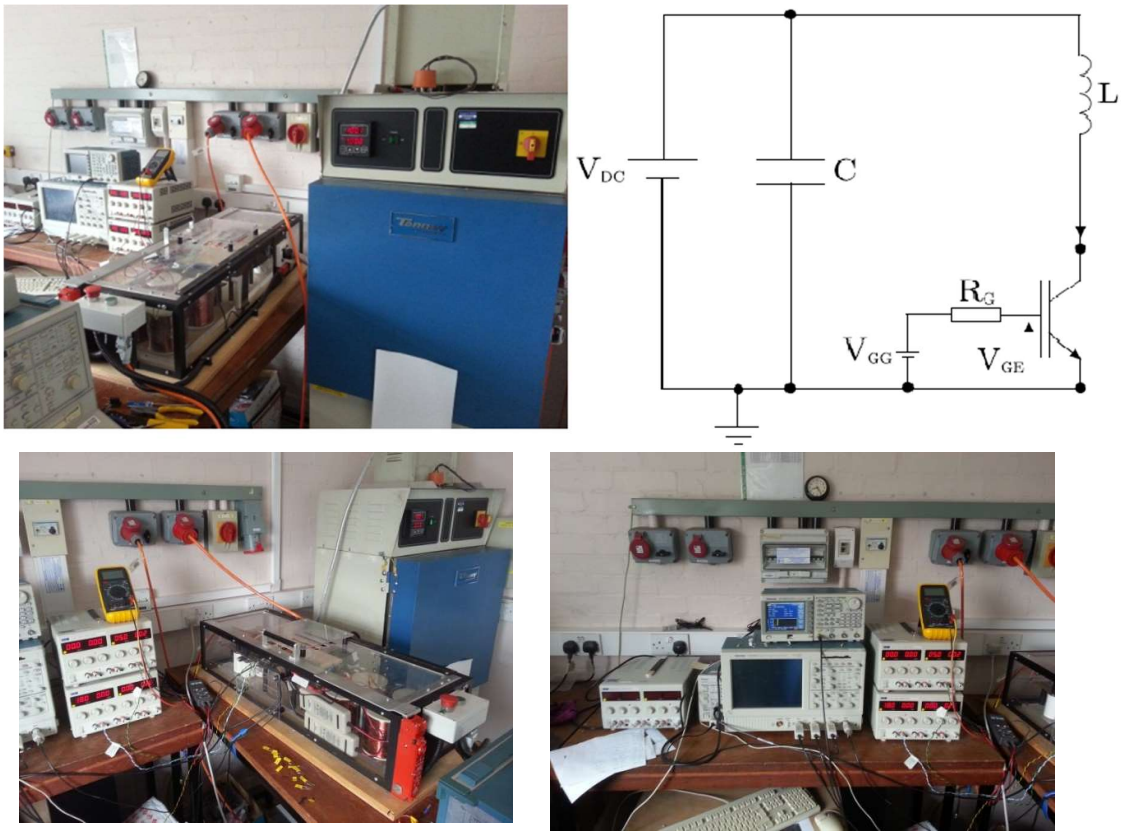


Figure 4.4-1 Experimental set-up showing unclamped inductive switching test and the circuit schematic

When the device under test (*DUT*) is switched on, the inductor is charged to the peak avalanche current which is proportional to the duration of the gate pulse. When the DUT is switched off, the current flowing through the inductor is interrupted, thereby causing the inductor to force current through the DUT. Since the DUT is off, current flows from the drain to the source through avalanche mode conduction. The drain-source voltage rises to a value that reaches the breakdown voltage as the current flows through the device[48, 55]. Figure 4.4-2 shows

experimental measurements of the gate-source voltage (V_{GS}), the drain-source current (I_{DS}) and the drain-source voltage (V_{DS}) as functions of time for a SiC MOSFET undergoing UIS

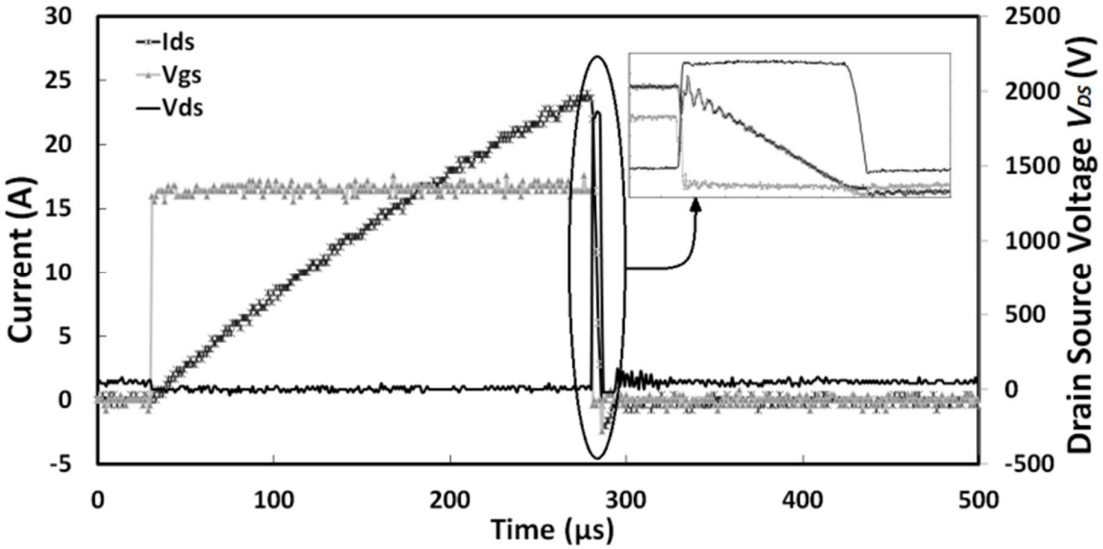


Figure 4.4-2 V_{GS}, V_{DS} and I_{DS} as functions of time for a SiC MOSFET under unclamped inductive switching

The devices used in the experiments were the 1.2 kV/24 A CREE SiC MOSFET with datasheet reference CMF10120D and the 1.2 kV/30 A Fairchild silicon IGBT with datasheet reference FGA15N120ANTD. The test was conducted at six different temperatures namely -25, 0, 25, 50, 75 and 100 °C. The performance of the device was examined under two different avalanche currents (24 A and 35 A). The 35 A test exceeds the maximum forward current rating of the SiC MOSFET by 40% and the maximum current rating of the IGBT by 16% thereby putting the SiC MOSFET under more electrothermal stress. Figure 4.4-3 shows the drain-source voltage of the SiC MOSFET under UIS at the rated current for different temperatures.

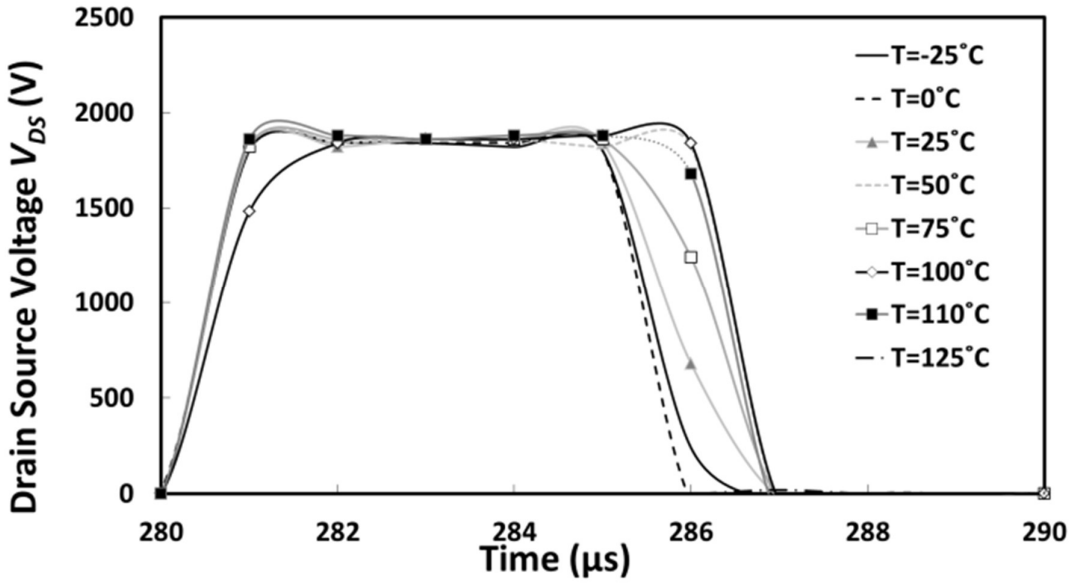


Figure 4.4-3 Drain-source voltage for the SiC MOSFET under UIS at different temperatures. Test current I_L= 24

At Figure 4.4-3 the voltage of the device under avalanche is presented. The drain source voltage is the breakdown voltage of the device. In this graph devices went into avalanche but none of them failed

4.4.2. Avalanche Performance using a different set up

A second set of tests were conducted using CREEs SiC MOSFET (CMF10120D), Fairchild's Si IGBT (FGA15N120ANTD) and IXYS Si MOSFET (IXFX20N120). All of the devices have a similar voltage and current rating. The tests were conducted using four different inductors 1.2 mH, 2.2mH, 4.8 mH and 9.5 mH. The devices were placed in an environmental chamber so we can simulate different ambient temperatures and define their importance. The tests were conducted at -25˚C, 0 ˚C, 25˚C, 50 ˚C, 75 ˚C and 125 ˚C. In literature it is common to use the device under test (DUT) to charge the inductor that will store the energy required to drive the device into avalanche. Two different circuits were used to determine if there is a major difference using the DUT as the charging element. The first is illustrated in Figure 4.3-3 and the second in Figure 4.4-4.

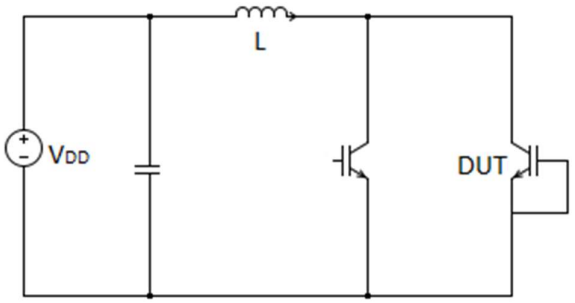


Figure 4.4-4 Circuit with DUT not charging the inductor

The experimental rig circuit diagram shown in Figure 4.3-3 is for avalanche measurements where the DUT is used to charge the inductor prior to avalanche mode conduction. The DUT is switched on thereby charging the inductor. After the DUT is switched off, the inductor discharges the stored current into the DUT. Figure 4.4-4 shows a set-up where a high voltage device is used to charge the inductor instead of the DUT. In the experimental rig circuit diagram shown in Figure 4.4-4, the DUT is not switched on prior to the avalanche test there is current going through it so the device is not heated due to conduction. Any stress then will be solely due to avalanche.

4.5. Analysis of the measurements

4.5.1. Measurements with conventional topology

4.6.1.1. Avalanche Performance at Fixed Currents

Figure 4.5-2 illustrates the collector-emitter voltage of the IGBT under UIS whereas Figure 4.5-3 displays the collector-emitter current of the IGBT under UIS. The SiC MOSFET demonstrates temperature invariant characteristics and withstands all temperatures, whereas the silicon IGBT does not withstand the avalanche current at 100 °C as can be seen in Figure 4.5-2 and Figure 4.5-3. In Figure 4.5-2 the V_{CE} of the IGBT collapses to zero at the moment the short circuit across the device occurs. In Figure 4.5-3 the current through the IGBT at 100

^{0}C rises uncontrollably, thereby indicating BJT latch-up. Subsequent tests on the device show that all the terminals were short circuited and the device was damaged.

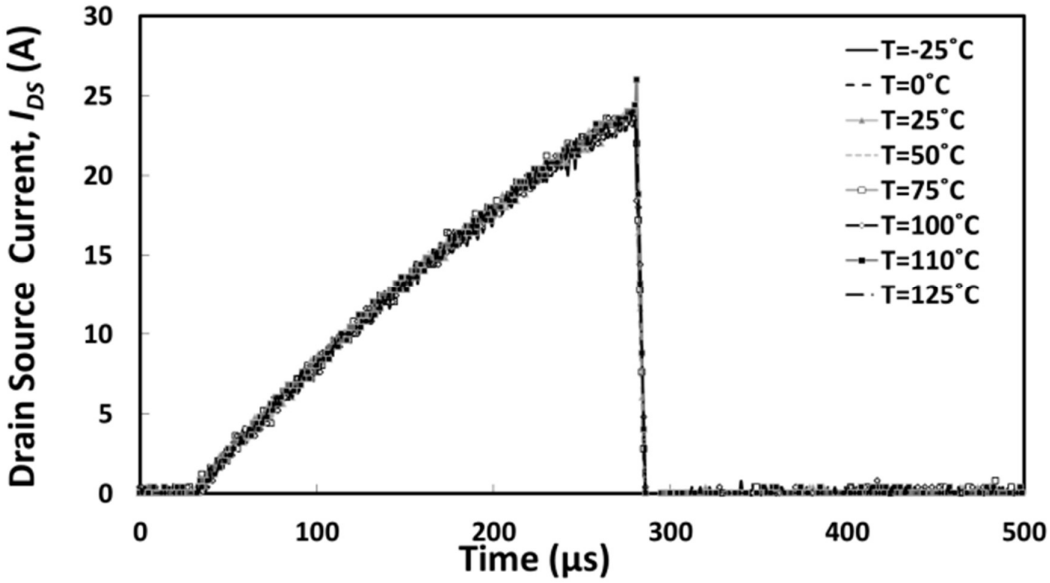


Figure 4.5-1 Drain-source current for the SiC MOSFET under UIS at different temperatures. Test current I_L= 24A

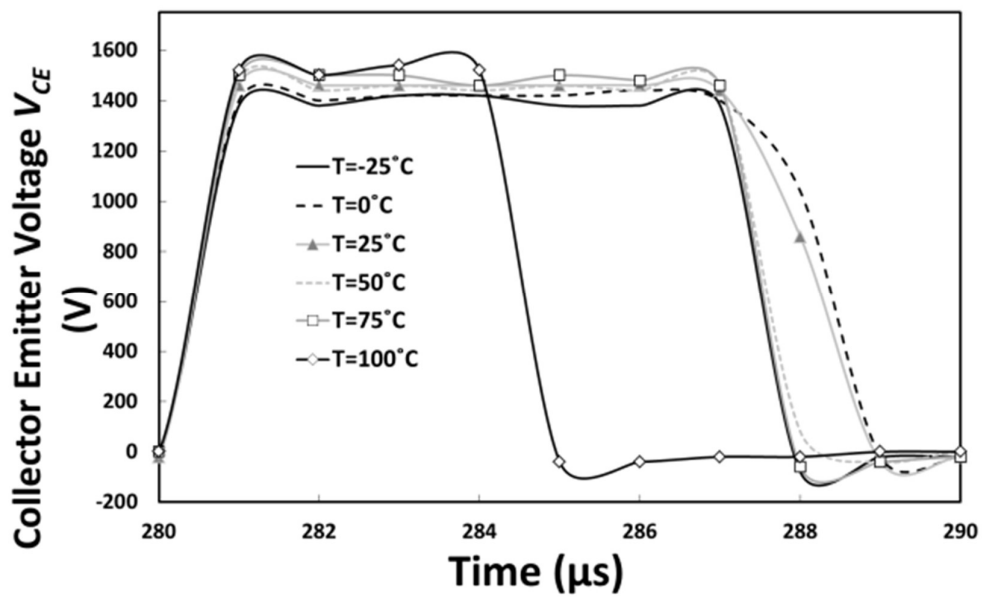


Figure 4.5-2 Collector-emitter voltage for the Si IGBT under UIS at different temperatures. Test current I_L= 24A

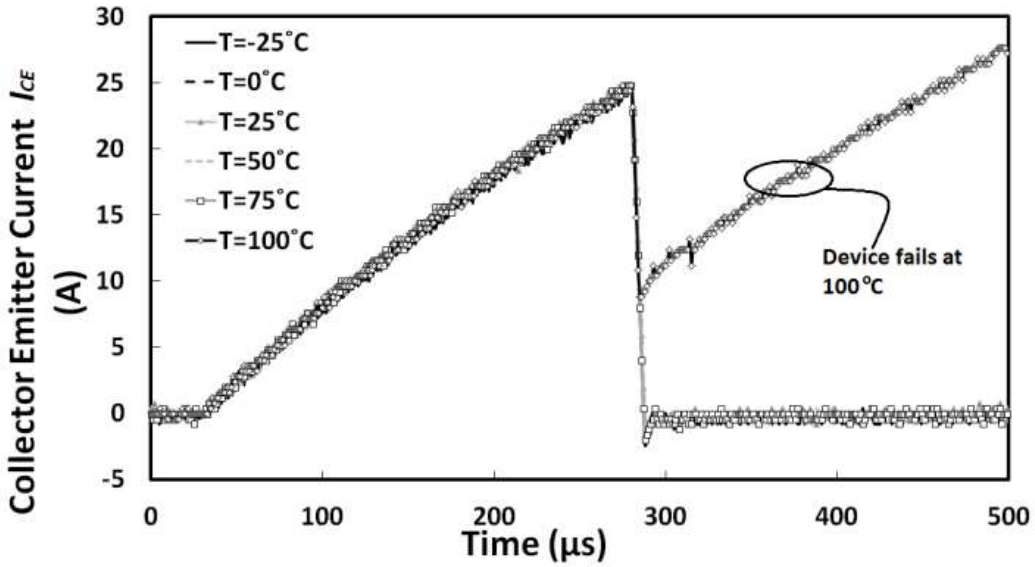


Figure 4.5-3 Collector-emitter current for the Si IGBT under UIS at different temperatures. Test current I_L= 24A

Next, the SiC MOSFET was tested at 40% beyond its current rating whereas the IGBT was tested at 16% beyond its current rating in order to ascertain the electrothermal ruggedness. Figure 4.5-4 shows the avalanche current characteristics of the SiC MOSFET under different temperatures. The MOSFET withstands the test at the low temperature measurements (-25 and 0 °C). For temperatures above 25 °C, the current rises and is limited by the power supply i.e. the MOSFET goes into thermal runaway. Subsequent tests on the devices showed that they are shorted between all three terminals indicating that the devices had failed. The mechanism behind the temperature dependency of the devices ability to withstand UIS can be explained by Figure 4.3-2. Figure 2.7-1, Figure 2.7-2 and Figure 4.5-5 Drain-source voltage for the SiC MOSFET under UIS at different temperatures showing BJT latch-up above 0 °C. Test current I_L= 35Ashows the corresponding drain-source voltage (V_{DS}) where it can be seen that V_{DS} falls to zero more quickly as the temperature is increased. This occurs as a result of the fact that the voltage across the device collapses once the bipolar has latched.

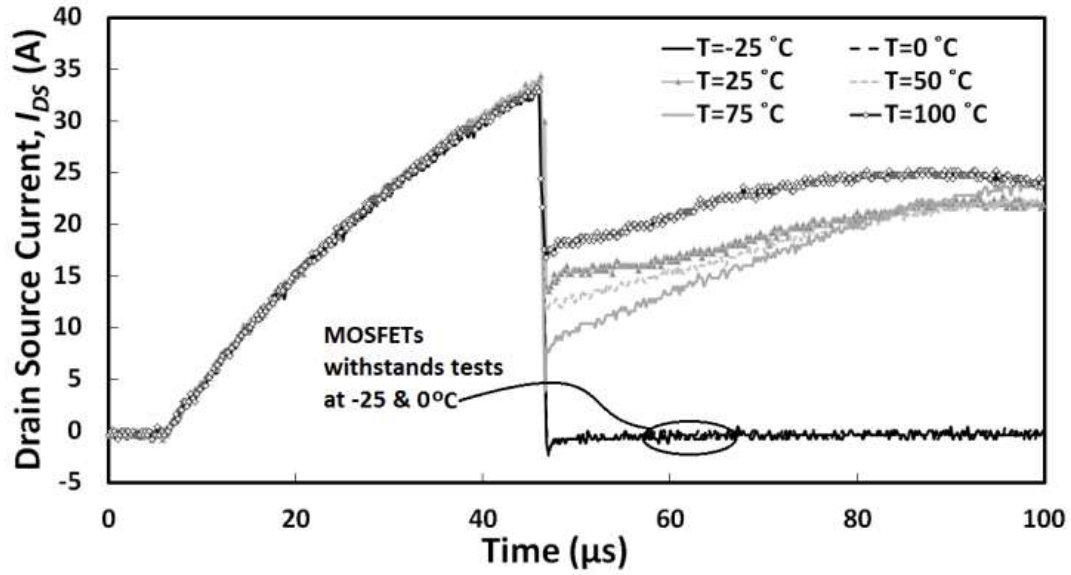


Figure 4.5-4 Drain-source current for the SiC MOSFET under UIS at different temperatures showing BJT latch-up above 0 °C. Test current I_L= 35A

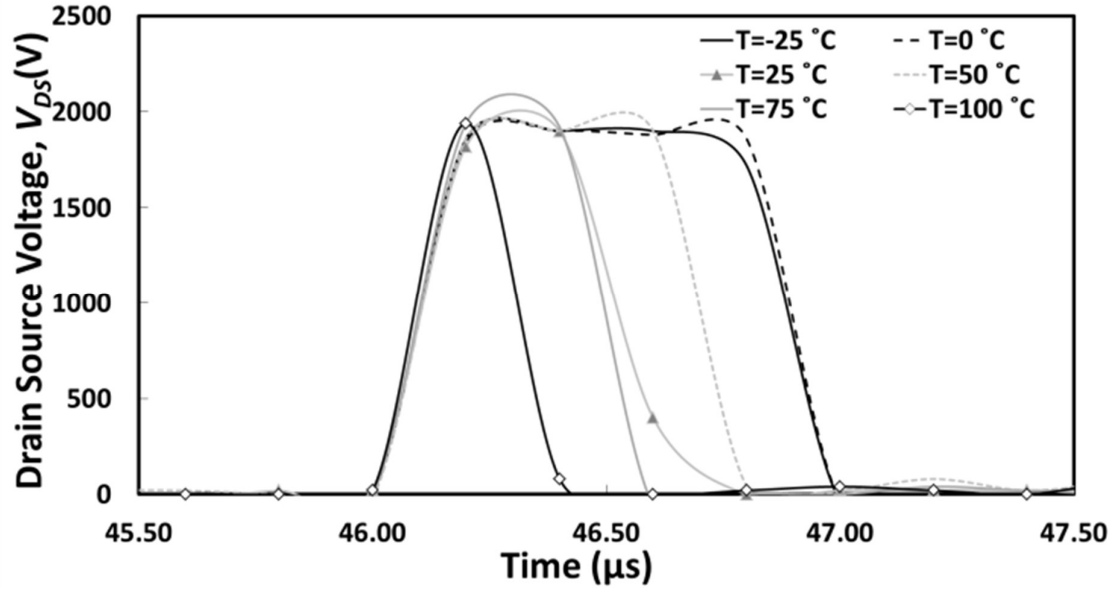


Figure 4.5-5 Drain-source voltage for the SiC MOSFET under UIS at different temperatures showing BJT latch-up above 0 °C. Test current I_L= 35A

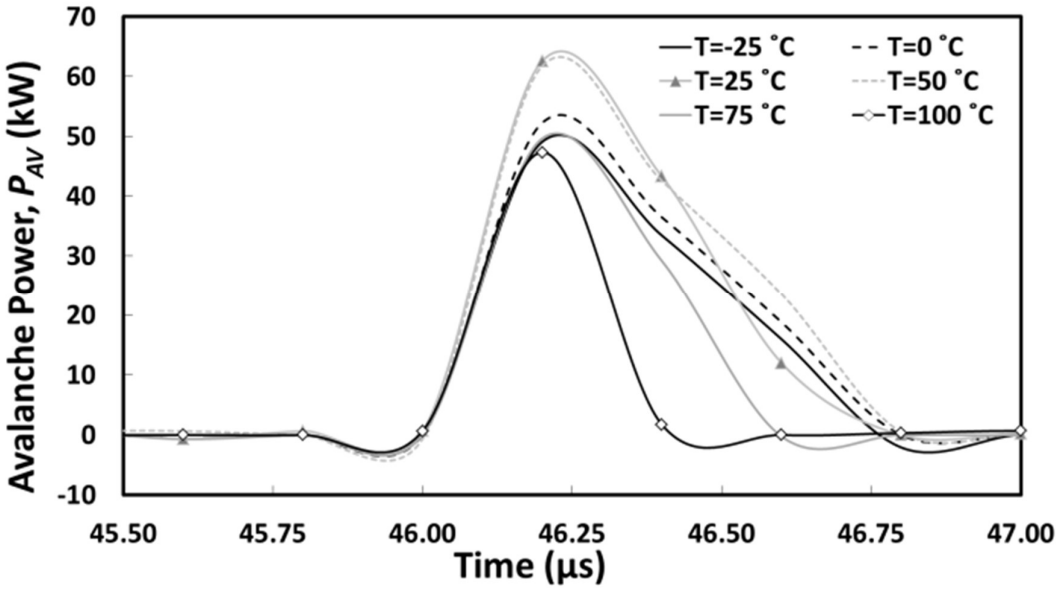


Figure 4.5-6 Avalanche power dissipated in the SiC MOSFET. Test current I_L= 35A

Figure 4.5-6 presents the avalanche power dissipated by the SiC MOSFET at different ambient temperatures. The amount of power dissipated by the device before the onset of the BJT latch-up increases as the temperature decreases. This can be explained by the fact that dissipated power contributes to temperature excursions within the device, hence, when the device starts at a lower ambient temperature there is more headroom to dissipate power before bipolar latch-up, the device needs to reach a critical temperature to latch up and fail. The dT of the temperature increase due to avalanche mode conduction is the same and depends on the avalanche energy. If the starting temperature is lower this dT will not be enough for the device to reach that critical temperature that destroys it.. Three previous pictures are the experimental validation of Figure 2.7-2 and Figure 2.7-3. The model developed for BJT latch-up in 2.7.

Figure 4.5-7 displays the collector-emitter current of the silicon IGBT under UIS conditions with 35 A maximum avalanche current. It can be seen that unlike the SiC MOSFET, the silicon IGBT does not withstand the test at any temperature. A trend can also be noticed from the IGBT current. The latch-up current (i.e. the current flowing through the device at the point when latch-up occurs) increases with increasing temperature. Figure 4.5-8 shows the

collector-emitter voltage of the IGBT under UIS conditions at all the temperatures. Similar to the MOSFETs, the voltage across the device collapses to zero once the device latches. Figure 4.5-9 shows the avalanche power dissipated before the on-set of thermal runaway. The amount of avalanche power dissipated before the parasitic BJT latch-up decreases with increasing temperature.

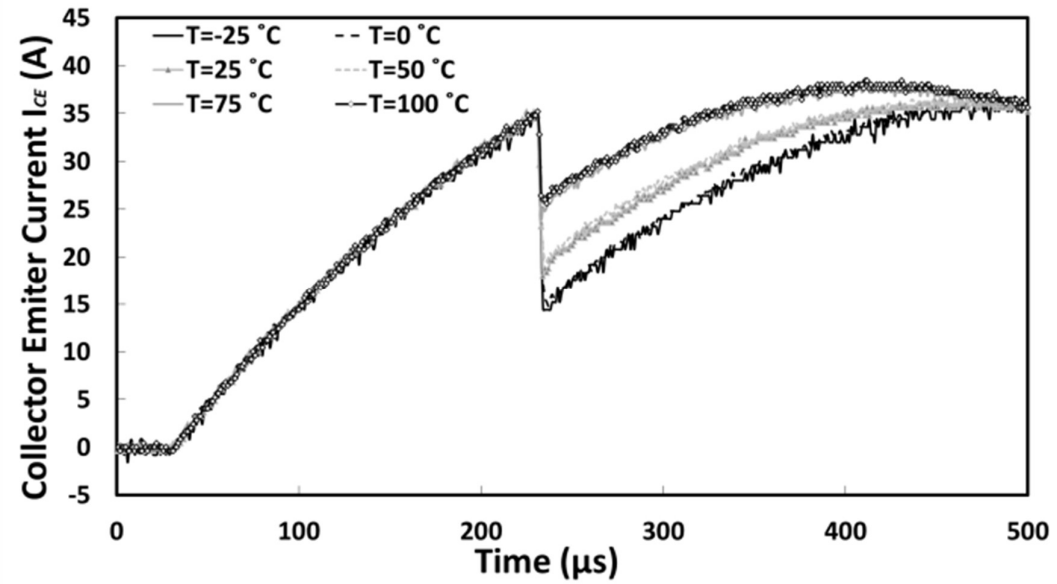


Figure 4.5-7 Collector-emitter current for the silicon IGBT under UIS at different temperatures. Test current I_L= 35A

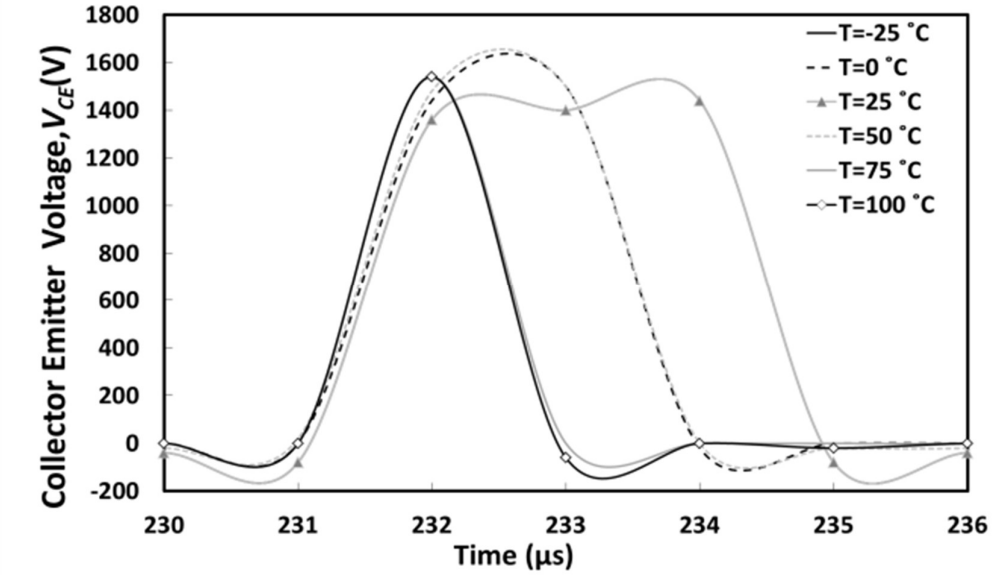


Figure 4.5-8 Collector-emitter voltage for the silicon IGBT under UIS at different temperatures. Test current I_L= 35A

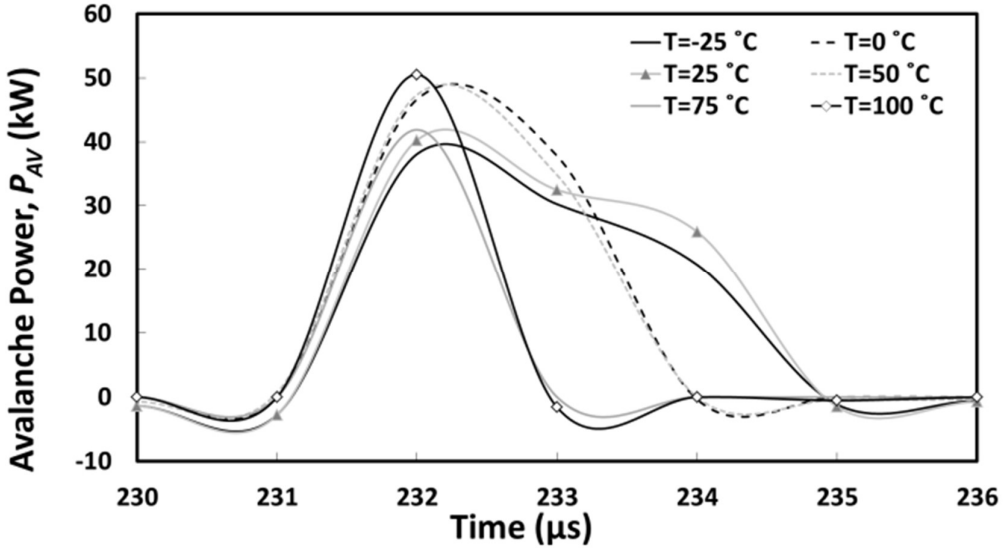


Figure 4.5-9 Avalanche power dissipated in the silicon IGBT. Test current I_L= 35A

Figure 4.5-10 shows the V_{CE} and V_{DS} characteristics of the IGBT and the MOSFET respectively during avalanche. It can be seen that the MOSFET has a higher breakdown voltage than the IGBT even though both devices are rated at 1.2 kV. Figure 4.5-11 shows that the gradient of the avalanche current is higher for the IGBT. This happens because of the higher breakdown voltage of the MOSFET since $t = \frac{LI_{AV}}{(B_{VDSS}-V_{DS})}$ where B_{VDSS} is the breakdown voltage, I_{AV} is the avalanche current and t is the time. Hence, Figure 4.5-11 shows that the avalanche current decreases as the avalanche duration increases.

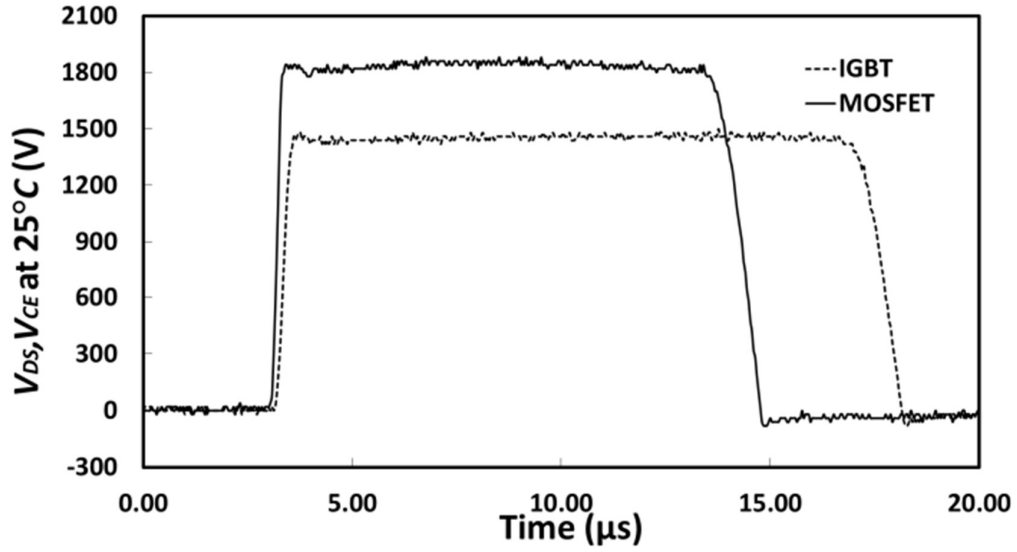


Figure 4.5-10 V_{DS} and V_{CE} for the IGBT and the MOSFET during avalanche mode conduction Test current I_L= 35A

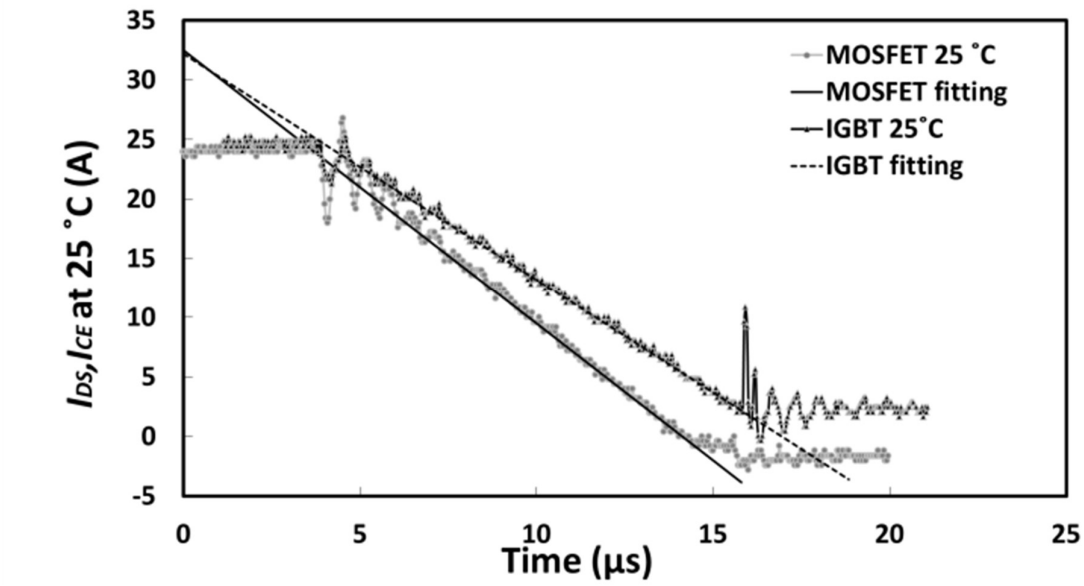


Figure 4.5-11 I_{DS} and I_{CE} for the IGBT and the MOSFET during avalanche mode conduction. Test current I_L= 35A

4.6.2. Maximum Avalanche Current Determination

The goal in this section is to determine the maximum avalanche current at a fixed temperature and fixed inductor (avalanche duration). This is done by increasing the pulse duration of the gate until device failure is initiated since the width of the gate pulse determines the peak avalanche current. The results of the measurements therefore show the peak avalanche current sustainable by the device. This test is conducted for both the SiC MOSFET and the silicon IGBT at different temperatures. Figure 4.5-12 shows the experimental measurements of different peak avalanche currents for the SiC MOSFET at room temperature. The measurements show that extending the gate pulse gradually will eventually cause device failure when the peak avalanche current is reached at that specific temperature.

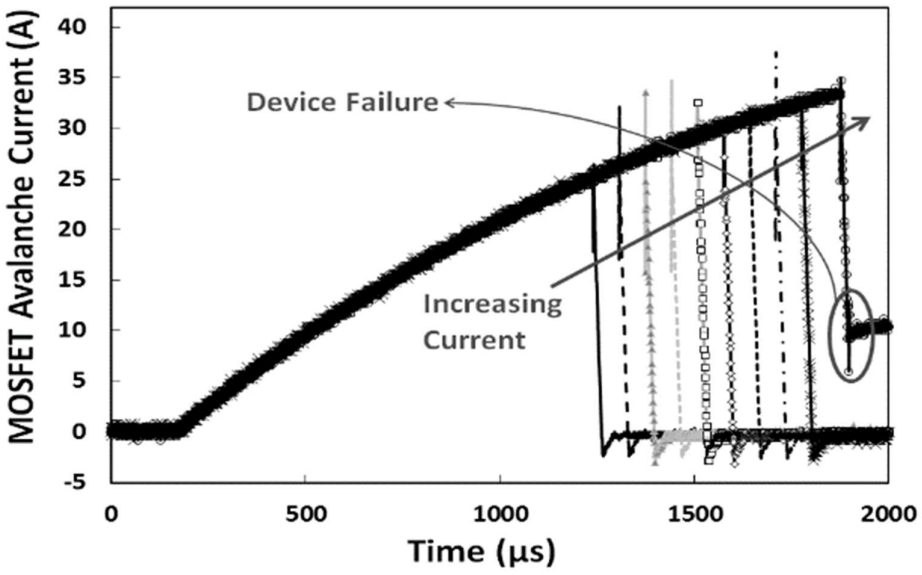


Figure 4.5-12 Avalanche current as a function of time for different gate pulses showing the maximum avalanche current for SiC MOSFET at ambient temperature.

Figure 4.5-13 illustrates the peak avalanche current when the Si IGBT fails at different temperatures. Figure 4.5-14 shows the equivalent results for the SiC MOSFET. It can be seen from both plots that the maximum avalanche current reduces with increasing temperature for reasons explained earlier. The total charging time of the MOSFET is smaller than that of the IGBT as a result of the smaller on-state resistance. Hence, less time is required for the device to reach a defined avalanche current.

Figure 4.5-15 displays the peak avalanche current sustained by the device before latch-up as a function of temperature for both the silicon IGBT and the SiC MOSFET.

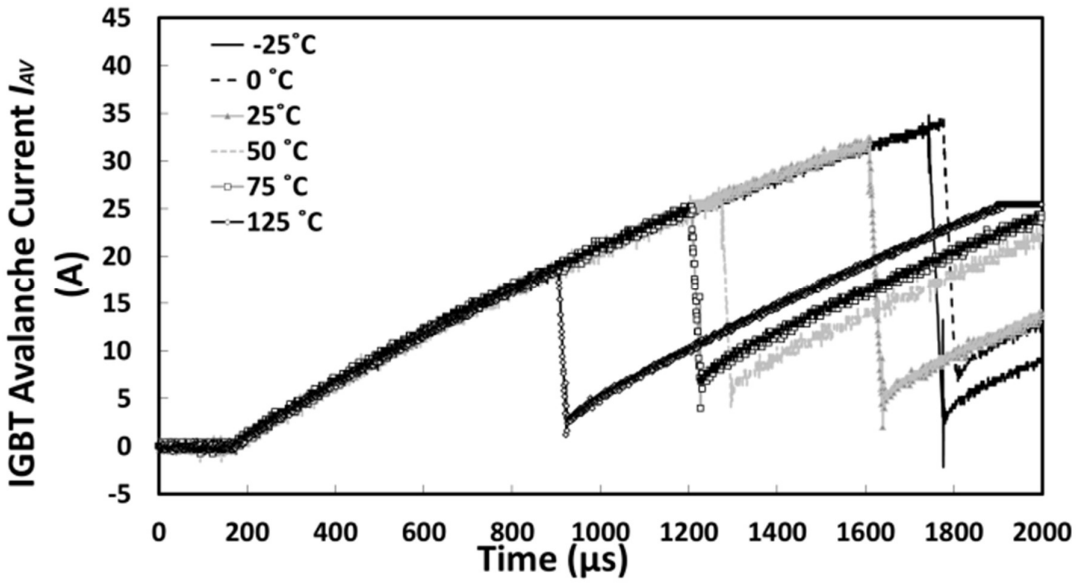


Figure 4.5-13 IGBT peak avalanche current as a function of time for different temperatures

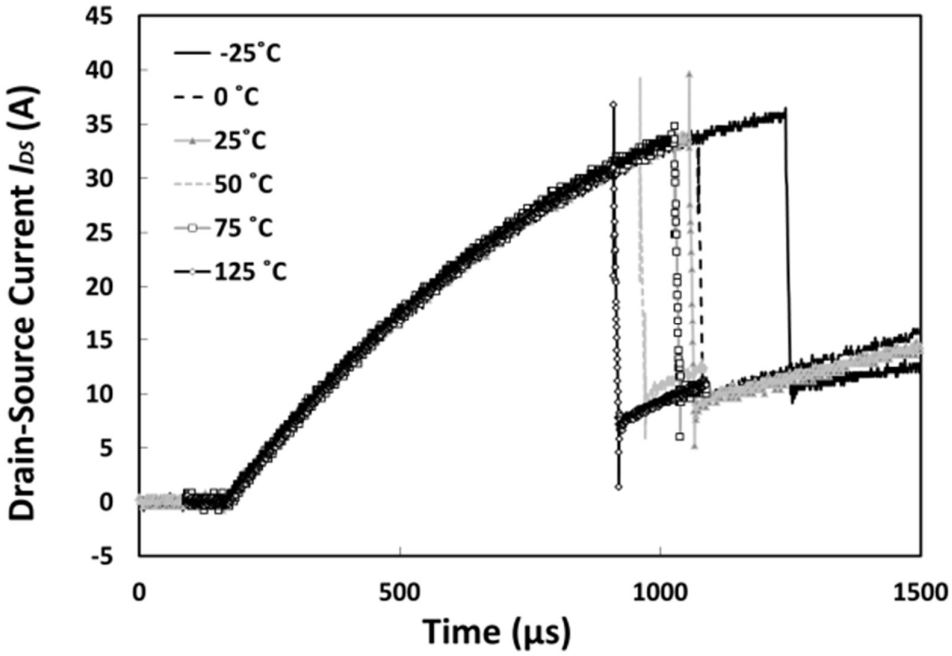


Figure 4.5-14 MOSFET peak avalanche current as a function of time for different temperatures

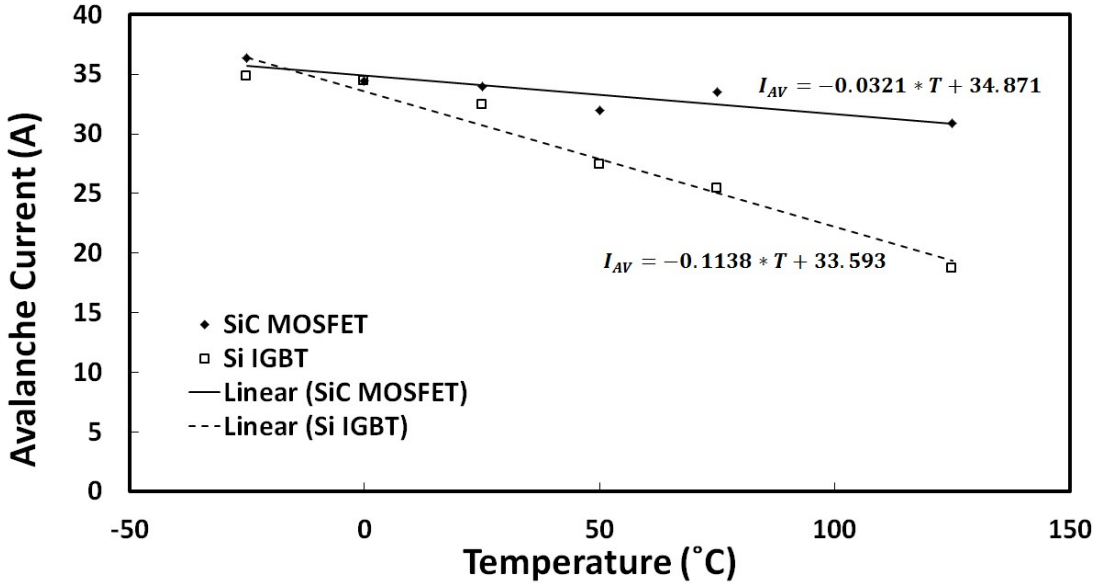


Figure 4.5-15 Peak avalanche current as a function of temperature for the MOSFET and the IGBT

It can be observed that the absolute value of the slope of the maximum I_{AV} vs. *temperature* is higher for the silicon IGBT thereby indicating a less reliable device at elevated temperatures, i.e. there is greater temperature dependency of electrothermal ruggedness in the IGBT than the MOSFET. The slope in Figure 4.5-15 is -0.114 A/^{0}C for the silicon IGBT and -0.031 A/^{0}C for the SiC MOSFET. The x-axis intercept of Figure 4.5-15 is an indication of the maximum operating temperature of the device. At this point, the elevated temperature causes enough thermal generation of carriers (through bandgap narrowing) that the carrier population is now equal to the background doping of the device i.e. the device ceases to be a semiconductor. The extrapolated maximum operating temperature (x-axis intercept) for the silicon IGBT and the SiC MOSFET is 295 ^{0}C (568 K) and 1086 ^{0}C (1360 K) respectively. However, in reality, the device will fail long before the theoretical point as a result of process imperfections leading to current crowding and heat non-uniformity. This means that some parts of the MOSFET die will be at much higher temperatures compared to others. Furthermore, packaging constraints will further limit the maximum junction temperature to a value significantly lower than what the semiconductor device is capable of. It can be seen from Figure 4.5-15 that the SiC device

has a much higher maximum operating temperature by virtue of wider bandgap. The intrinsic carrier concentration can be calculated for silicon and SiC from the following equations [35].

$$n_i = 3.87 \times 10^{16} T^{3/2} exp\left(-\frac{7.02\times10^3}{T}\right) \quad (4.5\text{-}1)$$

$$n_i = 1.7 \times 10^{16} T^{3/2} exp\left(-\frac{2.08\times10^4}{T}\right) \quad (4.5\text{-}2)$$

At 295 ^{0}C the calculated intrinsic carrier concentration for silicon is 2.25 × 1015 cm-3, whereas at 1086 ^{0}C the calculated intrinsic carrier concentration for SiC is 1.92 × 1014 cm-3. Hence, it is clear that the wide bandgap of SiC enables better electrothermal ruggedness since the thermally generated carrier concentration for SiC is less than that of silicon even when the ambient temperature is 3.5 times higher [56].

4.6.3. Tests with unconventional set up

4.6.3.1. DUT Charging the inductor

In Figure 4.5-16 the energy of the MOSFET at failure using different inductors and at different temperatures is presented, using different inductors changes the avalanche energy the device has to withstand. The inductor is used an energy storing element. Similar results for the IGBT are presented in Figure 4.5-17

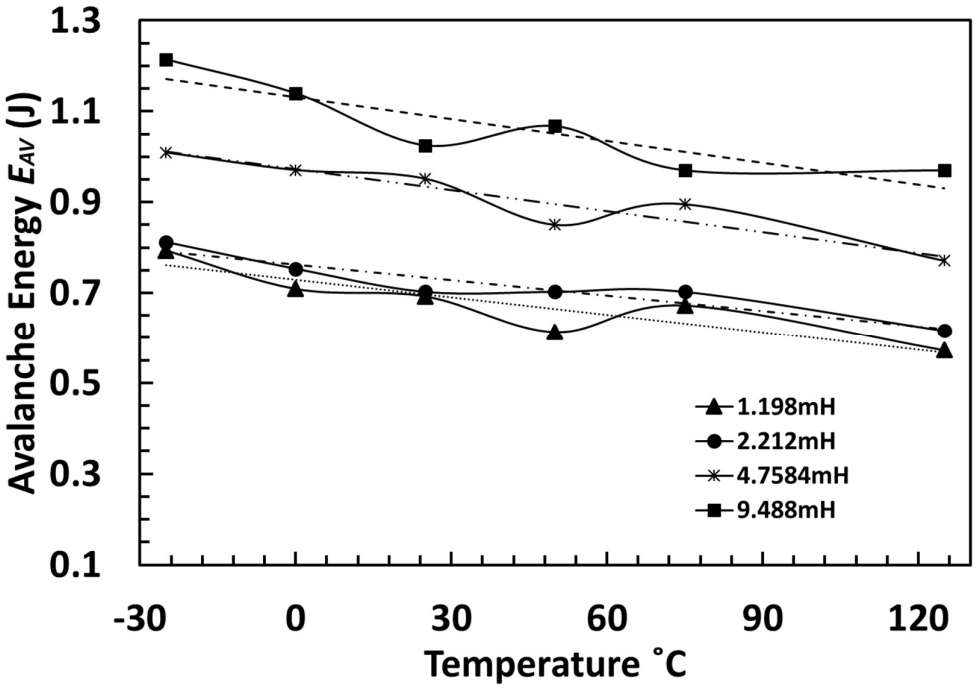


Figure 4.5-16. SiC MOSFET Energy at time of failure using different inductors

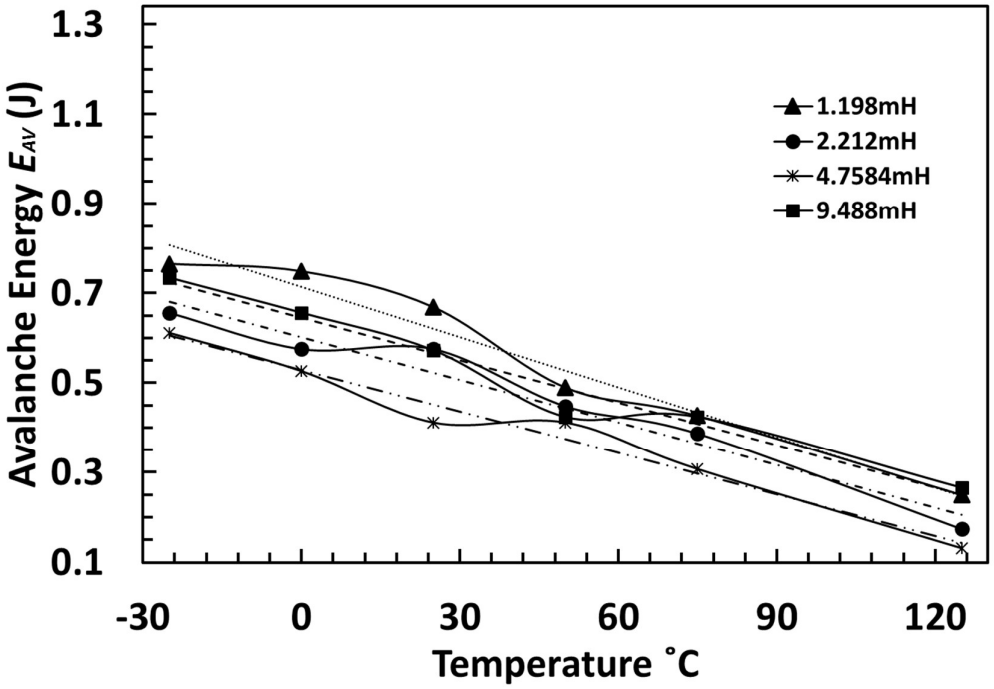


Figure 4.5-17 Si IGBT Energy at time of failure using different inductors

From the graphs we can see the SiC MOSFET can withstand much larger energies while the storage inductance increases. It is not the same case with the IGBT. The results don't show any major difference with different inductors. Also MOSFETs can handle temperature better compared to the IGBT but both behave worse when the temperature is increasing.

In the next graphs a comparison of the two architectures is presented for all the different inductances used

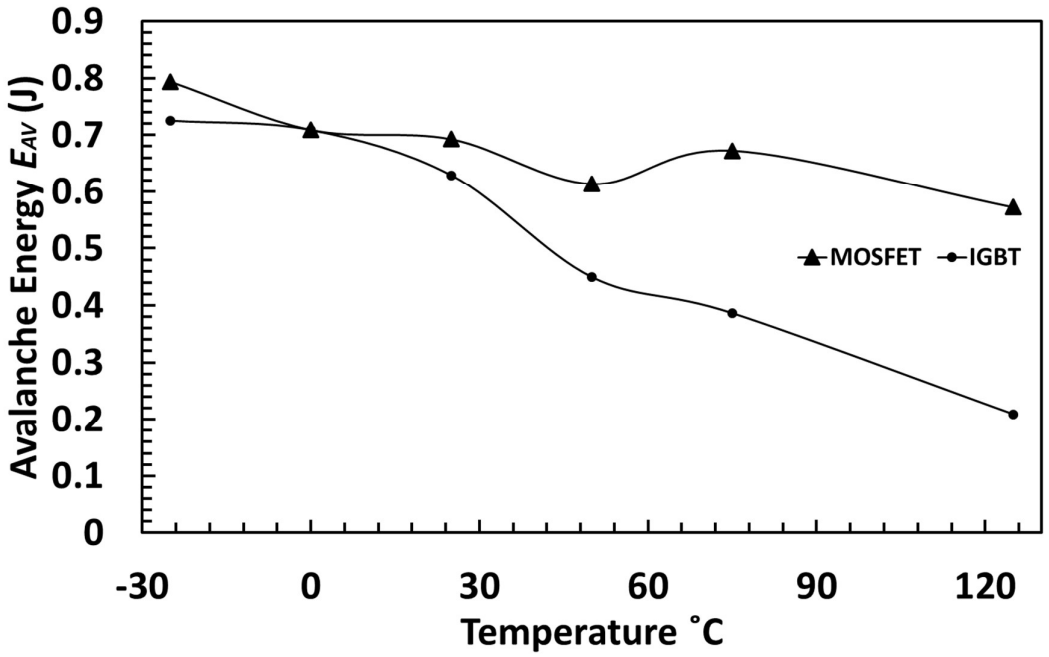


Figure 4.5-18 Energy Comparison between MOSFET IGBT using L=1.198mH

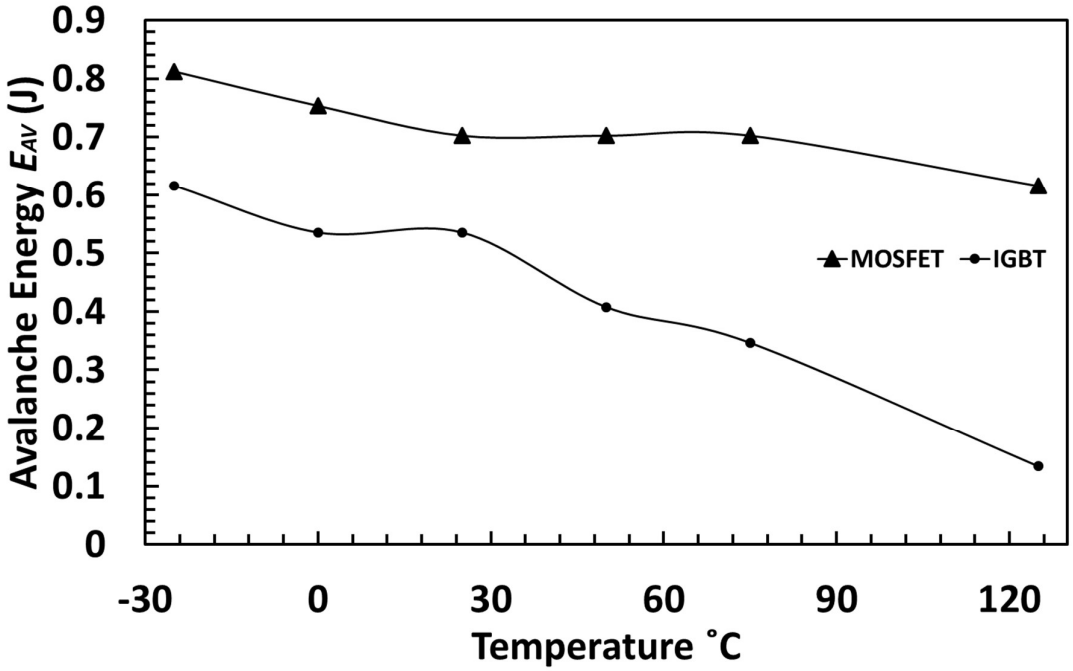


Figure 4.5-19 Energy Comparison between MOSFET IGBT using L=2.198mH

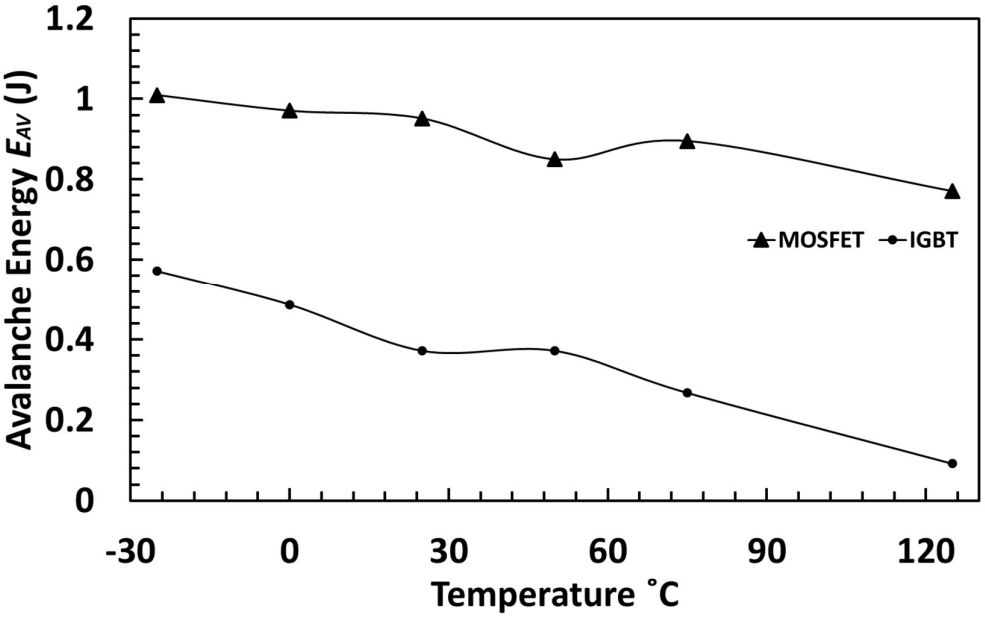


Figure 4.5-20 Energy Comparison between MOSFET IGBT using L=4.7584mH

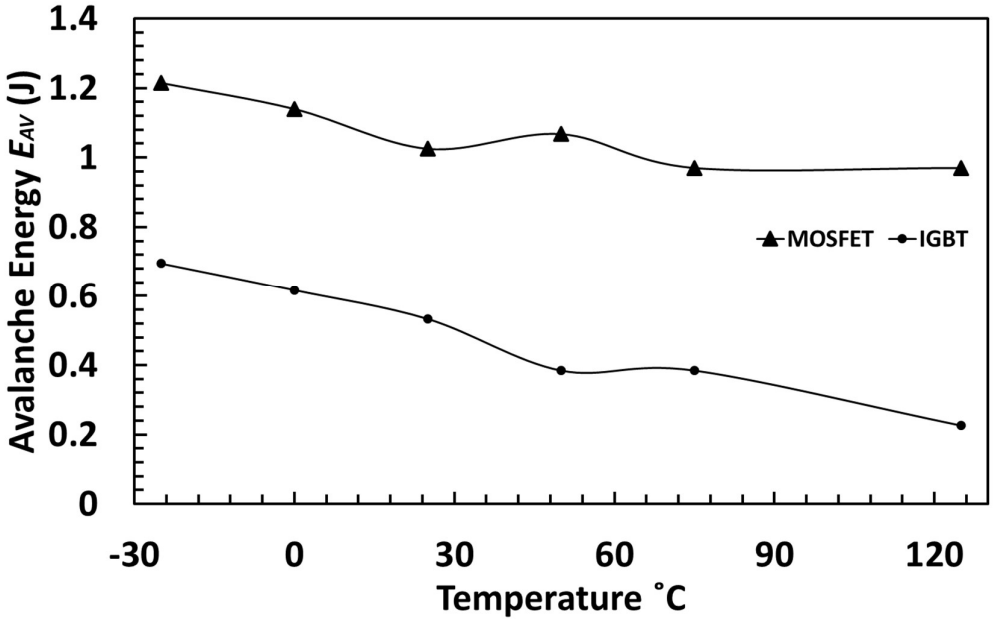


Figure 4.5-21 Energy Comparison between MOSFET IGBT using L=9.488mH

It is evident that the gap between the devices is increasing while the inductance is increasing. It is crucial to say that while the inductor becomes larger the duration of the avalanche increases but also the peak of the avalanche current is smaller.

4.6.3.2. DUT not charging the inductor

In the second part of the experiment, the avalanche inductor was charged using a high breakdown voltage device while the gate of the DUT was grounded. In other words, the DUT is never switched on. The circuit diagram used is shown in Figure 4.3-3. The high voltage device used was IXEL 40N400-N with a breakdown voltage of 4 kV and current capability of 90 A. Since the avalanche current will always flow through the device with the lower breakdown voltage rating, the high voltage device would not interfere with the avalanche measurements. The breakdown voltage of the device was not affected by grounding the gate and also the breakdown voltage between the IGBT and the MOSFET remained the same [57]. The benefit of using a different device to charge the inductor is because the DUT is not on

during charging the junction temperature doesn't increases due to conduction losses. The junction temperature in this case is a lot closer to ambient. The results for the avalanche current and the avalanche energy for the MOSFET are shown in Figure 4.5-22 and Figure 4.5-23 and for the IGBT in Figure 4.5-24 and Figure 4.5-25.

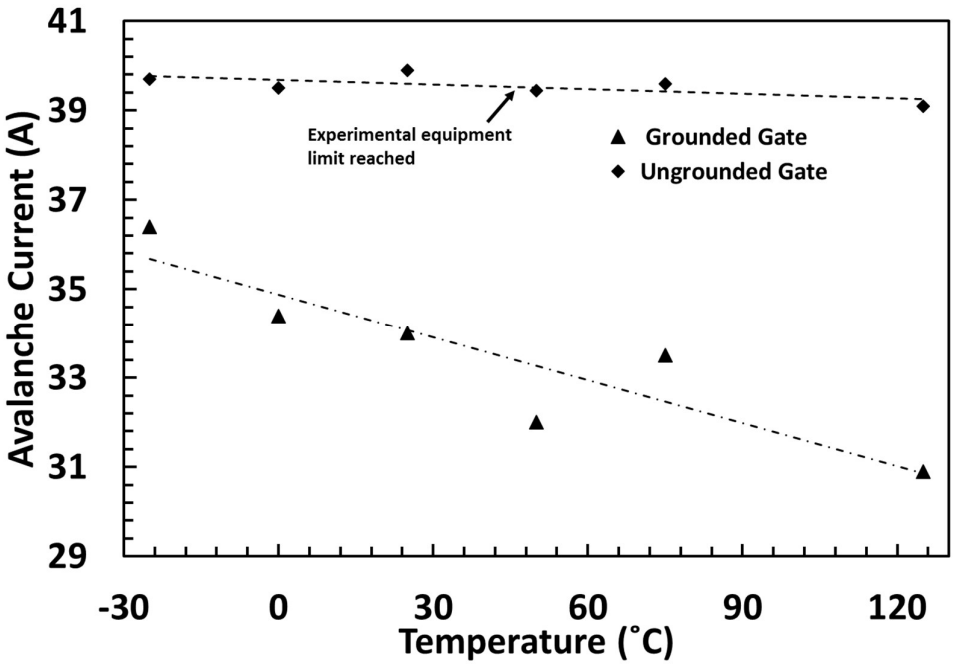


Figure 4.5-22 Comparison of I_{AV} between grounded and non-grounded gate

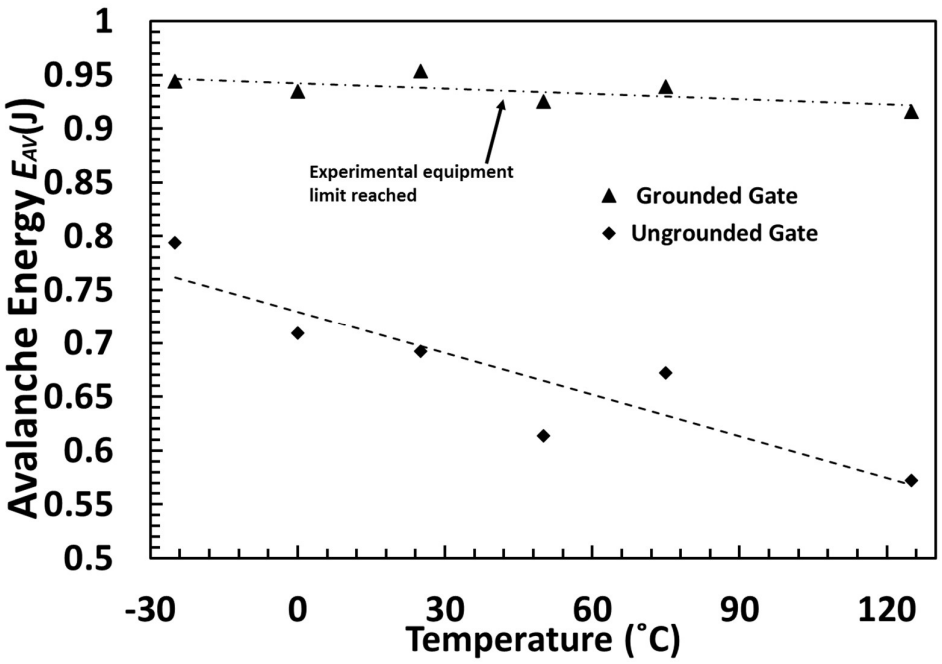


Figure 4.5-23 Comparison of E_{AV} between grounded and non-grounded gate

It is clear that there is a major difference between the two configurations. With the gate of the SiC MOSFET grounded, there was insufficient energy to trigger BJT latch-up and thermal runaway in the device, the reason this conclusion is made is due to the fact the device wasn't destroyed. The limits of the test equipment were reached. Results for the IGBT are shown in Figure 4.5-24 and Figure 4.5-25

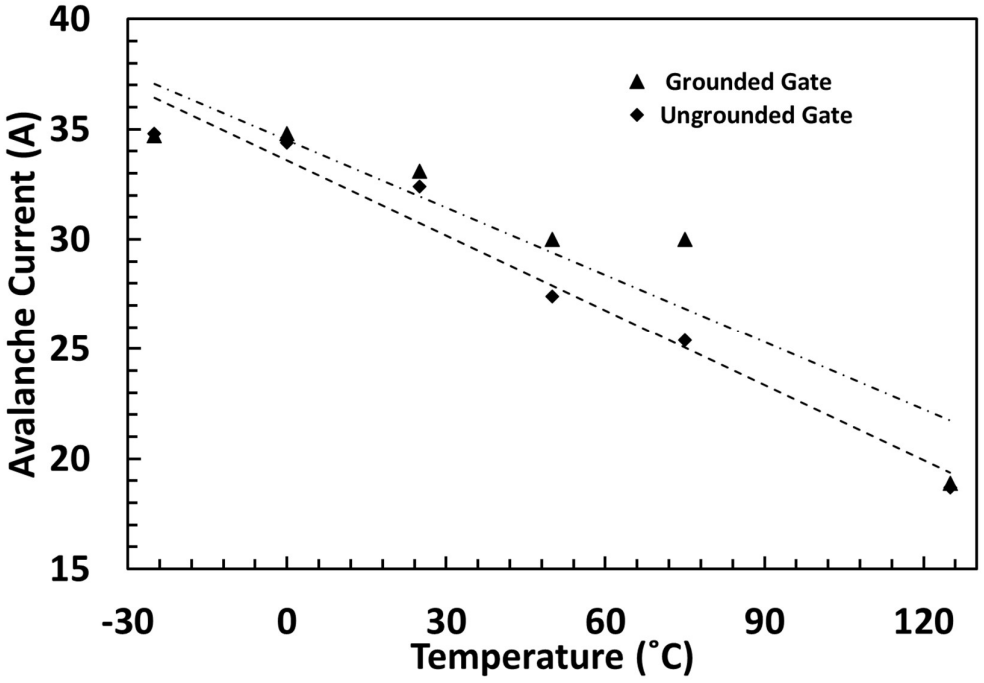


Figure 4.5-24 Comparison of I_{AV} between grounded and non-grounded gate

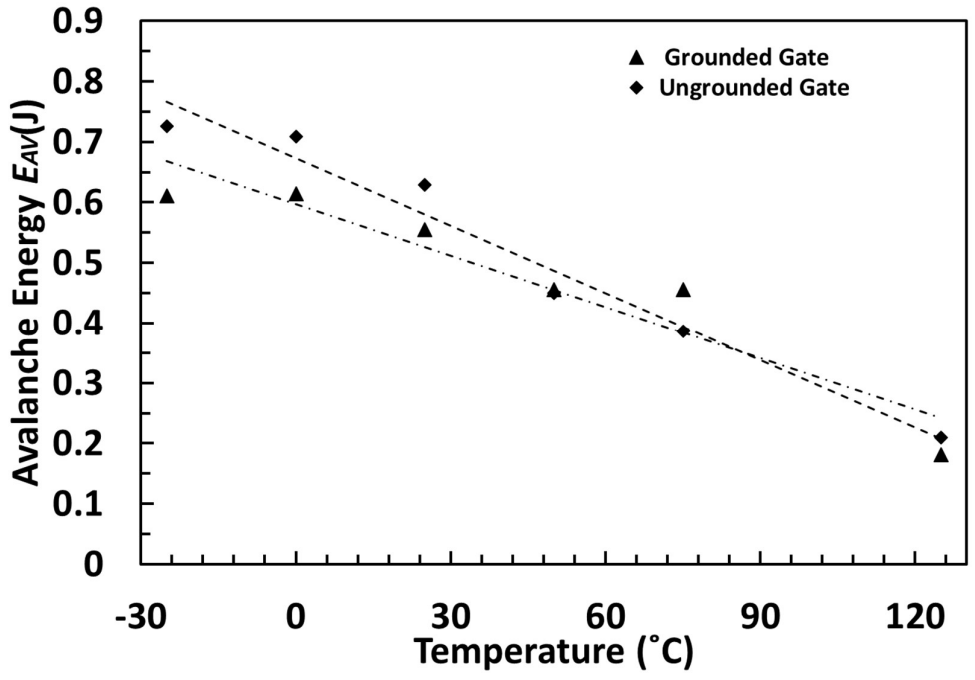


Figure 4.5-25 Comparison of E_{AV} between grounded and non-grounded gate

This was not the case with the silicon IGBT. Figure 4.5-24 shows the maximum avalanche current sustainable by the silicon IGBT as a function of temperature for the circuit

configuration shown in Figure 4.3-3 (ungrounded gate where the DUT charges the inductor) and Figure 4.4-4 (grounded gate where the DUT does not charge the inductor). Figure 4.5-25 shows the calculated avalanche energy as a function of temperature. As expected, higher temperatures reduce the avalanche capability. However, unlike the case of the MOSFET, there is not a substantial difference between the 2 tests. In other words, using the DUT to charge the inductor does not yield avalanche ruggedness results that are significantly less than using a higher voltage transistor to charge the inductor.

The drain-source voltage during avalanche is shown in Figure 4.5-26 for SiC MOSFET under both test conditions where it can be seen that the breakdown voltage does not change. Figure 4.5-27 shows a similar plot for the silicon IGBT. Figure 4.5-28 shows the drain-source voltage characteristics for the silicon IGBT and SiC MOSFET during avalanche where it can be seen that the breakdown voltage is higher for the SiC MOSFET and the avalanche duration is shorter. It should be noted that all the measurements are with the same inductor. The longer avalanche duration in the SiC MOSFET is due to the higher breakdown voltage. The breakdown voltage difference is the same as presented in [57].

Similar avalanche ruggedness tests have been carried out on 1.2 kV silicon MOSFETs the results of which as shown in Figure 4.5-29 with the other devices.

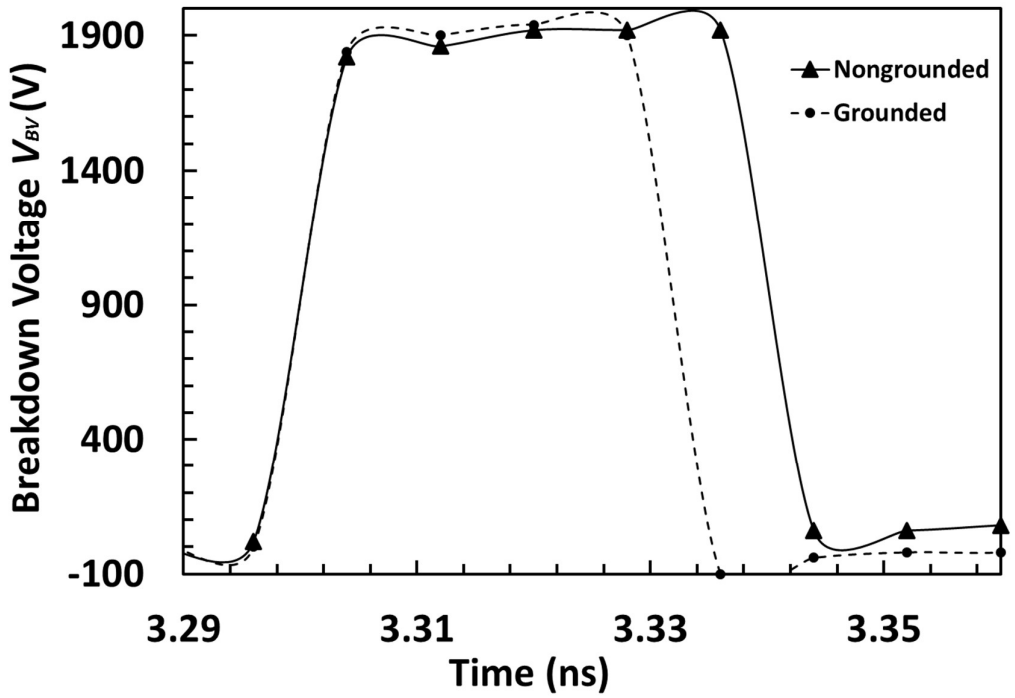


Figure 4.5-26 Breakdown voltage of MOSFET with both configurations

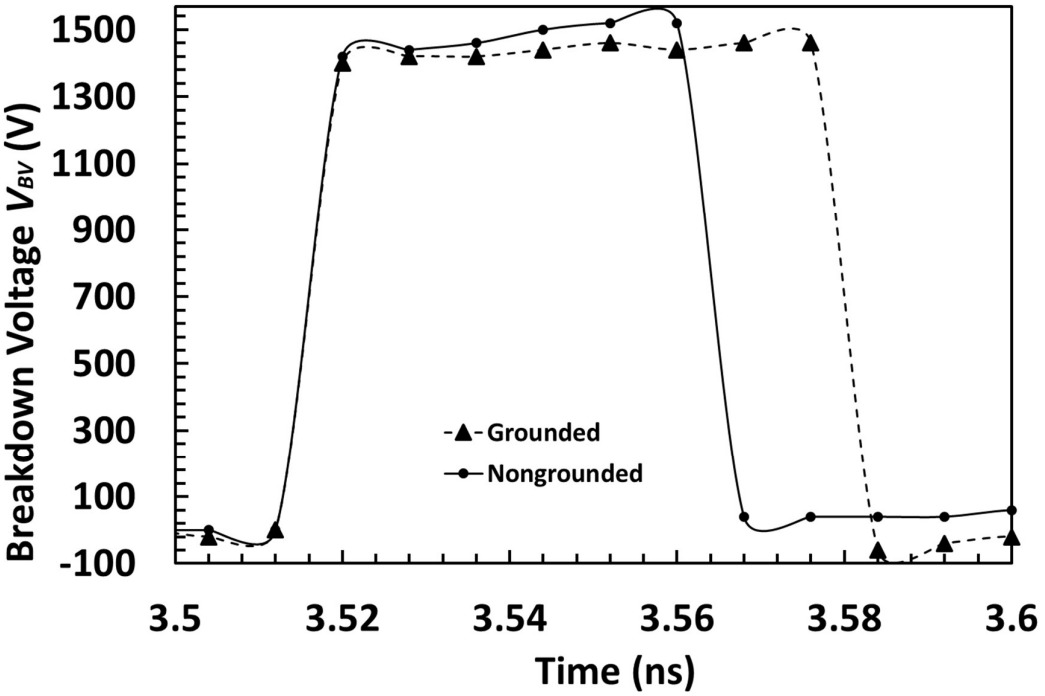


Figure 4.5-27 Breakdown voltage of IGBT with both configurations

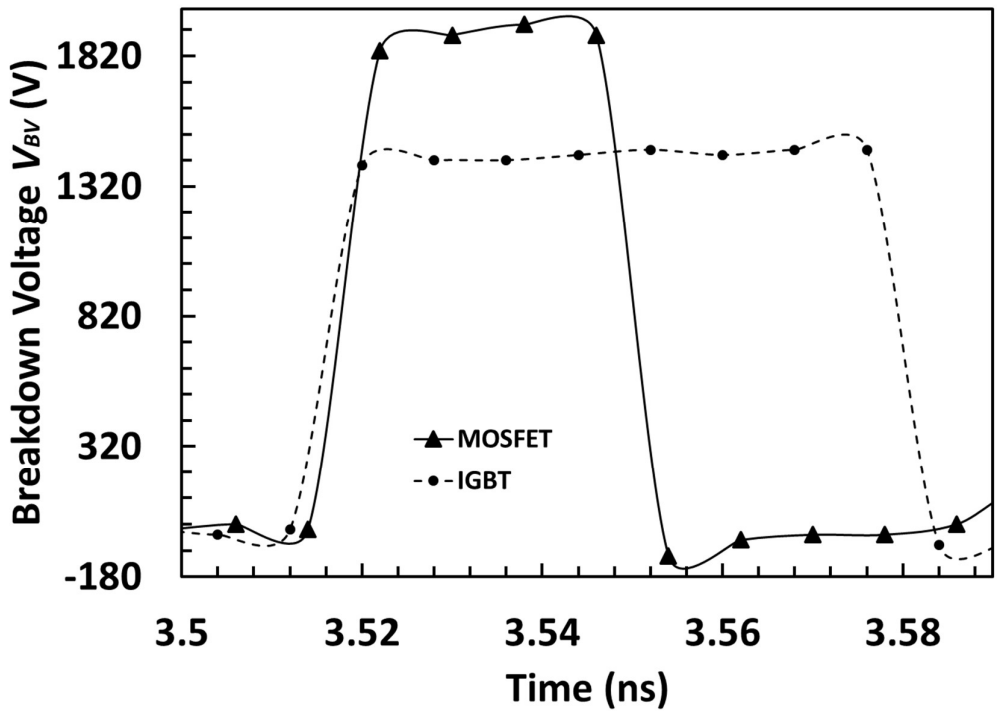


Figure 4.5-28 Breakdown voltage of IGBT and MOSFET with grounded gates on both devices

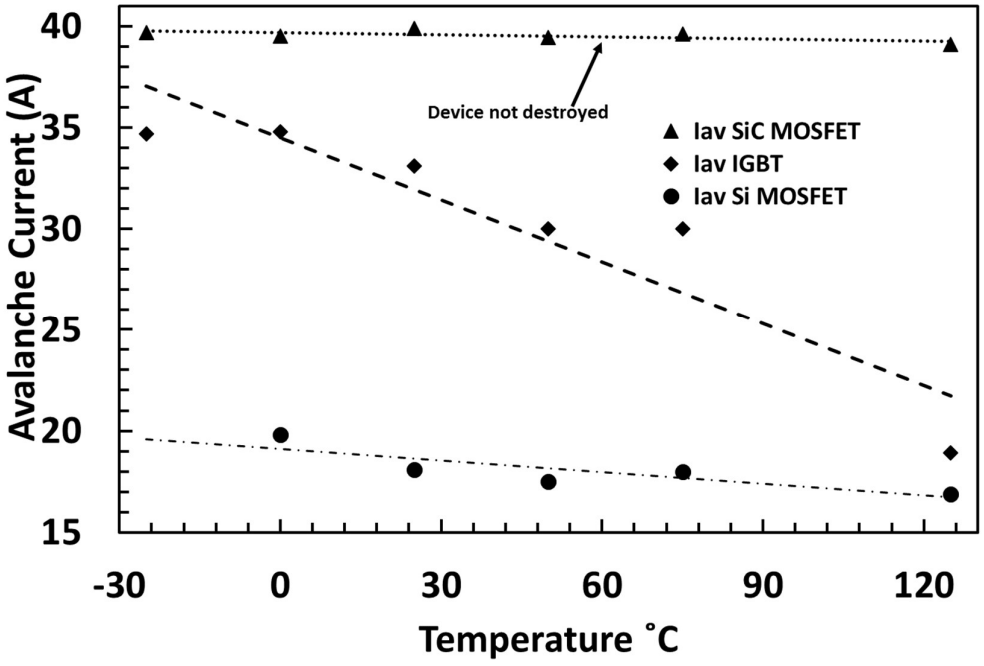


Figure 4.5-29 Avalanche current for SiC MOSFET, Si IGBT, Si MOSFET with grounded gates

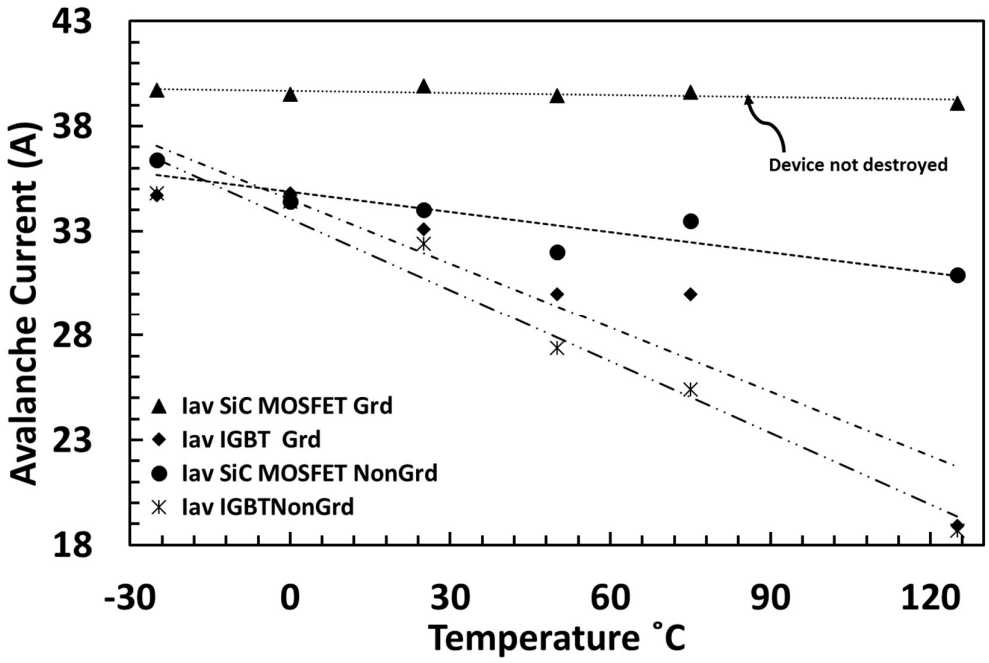


Figure 4.5-30 Avalanche current for SiC MOSFET, Si IGBT for both configurations.

In Figure 4.5-29, all of the measurements have been carried out on the 9.5 mH inductor with the DUT not used to charge the inductor. From Figure 4.5-29 it is evident that the most resilient device is the SiC MOSFET followed by the silicon IGBT and the Si MOSFET. The dependency of the avalanche ruggedness capability on temperature is more or less similar between the two MOSFETs probably due to the same architecture. The differentiating factor between the MOSFETs capability is the superior electrothermal capability of silicon carbide.

4.6.Junction Temperature Modelling by Finite Element Simulations

Finite element models have been developed to describe SiC MOSFET and silicon IGBT behaviour under avalanche mode conditions. ATLAS from SILVACO was used to investigate the electro-thermal behaviour of the MOSFET during avalanche. The SiC device in the simulation was optimized to yield a breakdown voltage of 1200 V by using an 8 μm depletion layer with a doping of $2X10^{16}$ cm^{-3}. The p-body doping and n-source was $1x10^{17}$ cm^{-3} and $2x10^{19}$ cm^{-3} respectively. The silicon IGBT is simulated with a drift layer doping of $1.1x10^{14}$

cm^{-3}, a p-body doping of $2.3x10^{17}$ cm^{-3} and a voltage blocking drift layer thickness of 100 μm. The circuit in the simulator was identical to the one used in the experiment. The results of the simulations are shown in Figure 4.6-1 to Figure 4.6-3 for both the MOSFET and the IGBT. Figure 4.6-1 illustrates the avalanche current as a function of time for the MOSFET and the IGBT. The ambient temperature of the simulation is 473 K and the avalanche current is 35 A. It can be seen from Figure 4.6-1 that the IGBT goes into latch-up whereas the MOSFET does not. Figure 4.6-2 illustrates the voltage across the device as a function of time for both the SiC MOSFET and the silicon IGBT. It can be observed that the IGBT has a higher voltage during the inductor charging period than the MOSFET. This is due to the higher on-state resistance of the IGBT as a result of the thicker drift layer compared to the SiC MOSFET, where the wide bandgap and high critical field means a thinner voltage blocking epitaxial layer is needed. The modelled characteristics of the voltage of the device during avalanche is identical to what is observed experimentally i.e. once the device goes into avalanche mode conduction, the voltage across the device rises to the breakdown voltage and if the device latches, the voltage across the device falls to zero as the current rises. Figure 4.6-3 shows the simulated maximum temperature of the device as a function of time during the inductor charging and the avalanche period.

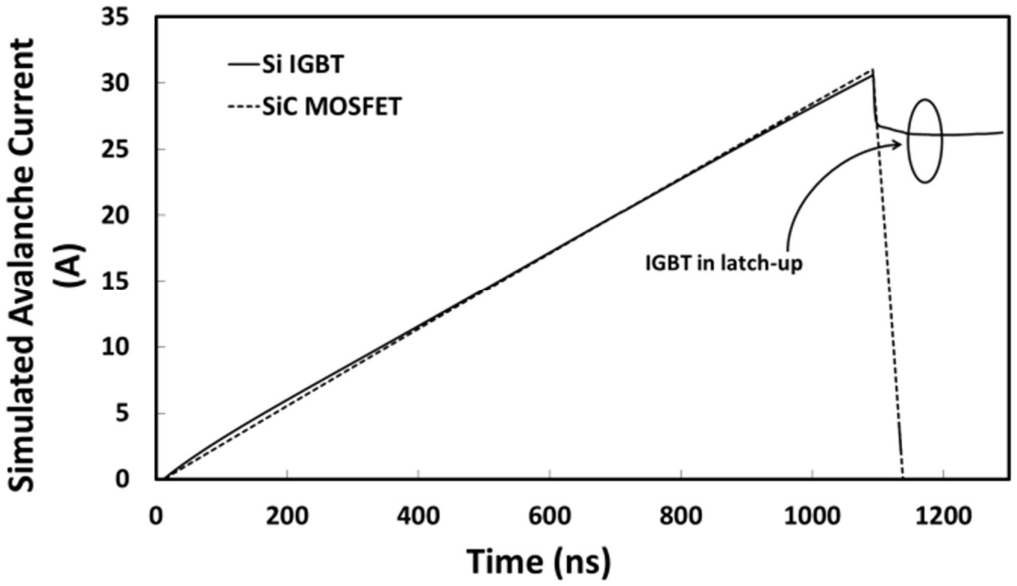


Figure 4.6-1 Simulated avalanche current as a function of time for the SiC MOSFET and the silicon IGBT

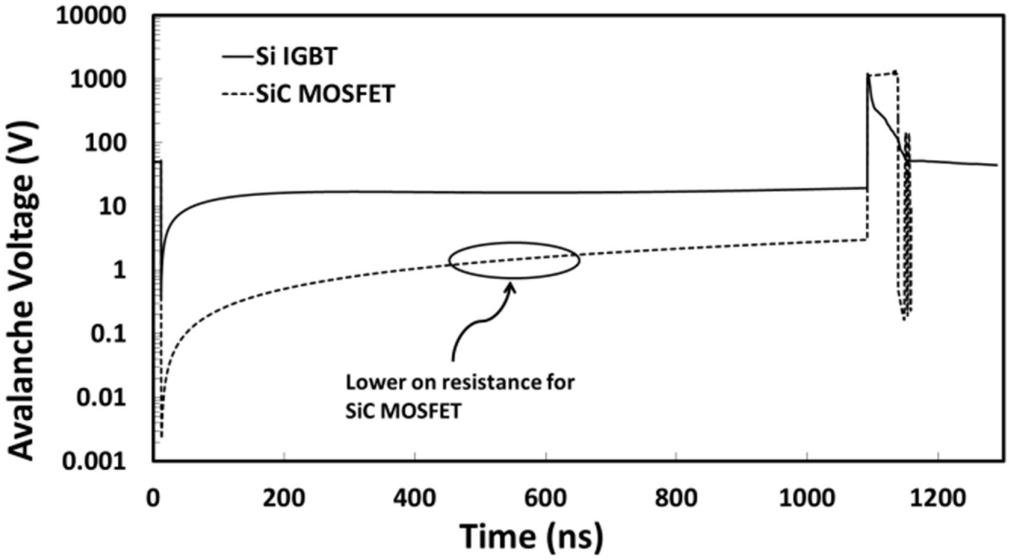


Figure 4.6-2 Simulated avalanche voltage as a function of time for the SiC MOSFET and the silicon IGBT.

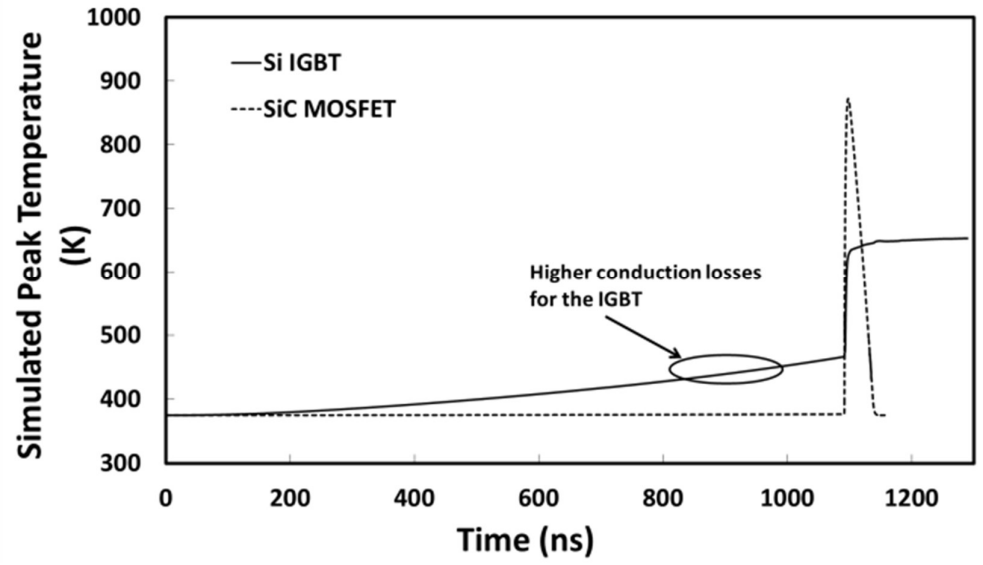


Figure 4.6-3 Simulated maximum temperature as a function of time for the SiC MOSFET and the silicon IGBT.

The IGBT shows a higher temperature rise during the inductor charging period as a result of the higher conduction losses compared to the SiC MOSFET. The rise of the SiC MOSFET temperature during avalanche is faster and the peak temperature is higher because of the smaller thermal time constant. The simulated SiC MOSFET will have a smaller thermal resistance (R_{TH}) because of the thinner epitaxial drift layer (thermal resistance increases with length in the direction of heat flow). SiC also has a thermal conductivity that is three times larger than silicon, hence, the thermal resistance would reduce even further. The SiC MOSFET will also have a smaller heat capacitance (C_{TH}) as a result of the smaller die mass. Therefore, the smaller thermal time constant ($R_{TH} \cdot C_{TH}$) means the rate of change of temperature with time will be higher, hence, the faster heating and cooling exhibited in Figure 4.6-3. It can also be seen in Figure 4.6-3 that the IGBT never cools down unlike the SiC MOSFET. Figure 4.6-4 displays more finite element simulations for the silicon IGBT during inductor charging and avalanche mode conduction at different ambient temperatures. It can be seen from Figure 4.6-4, that similar to the case of the experimental measurements, higher temperatures induce latch-up. Furthermore, in the finite element analysis the latch-up occurs approximately at 650 K which

is higher than what was extracted experimentally (568 K) by extrapolating the plots in Figure 4.5-15. This is expected since the simulation does not take into consideration process imperfections and packaging constraints.

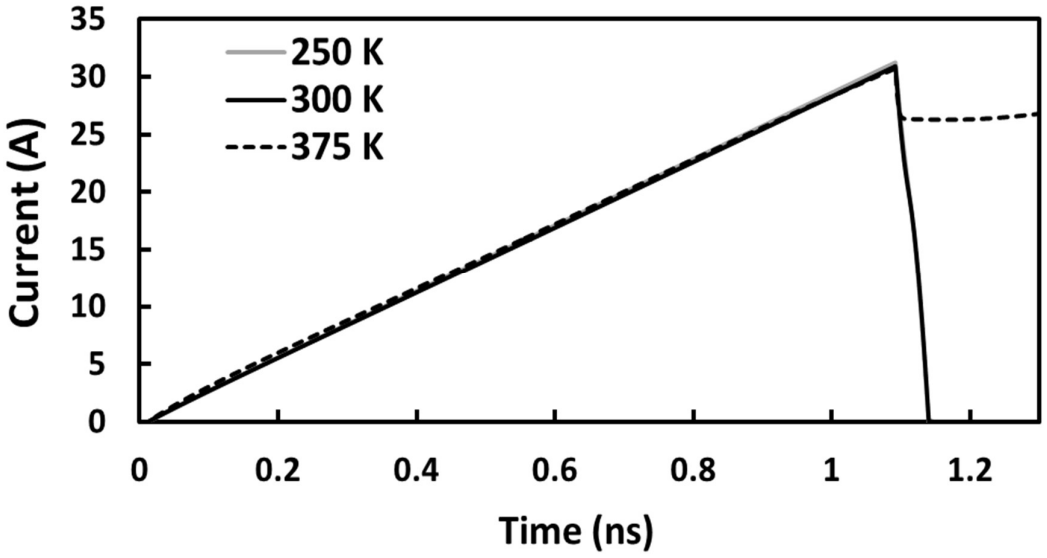


Figure 4.6-4 Simulated IGBT current during inductor charging and avalanche at different ambient temperatures.

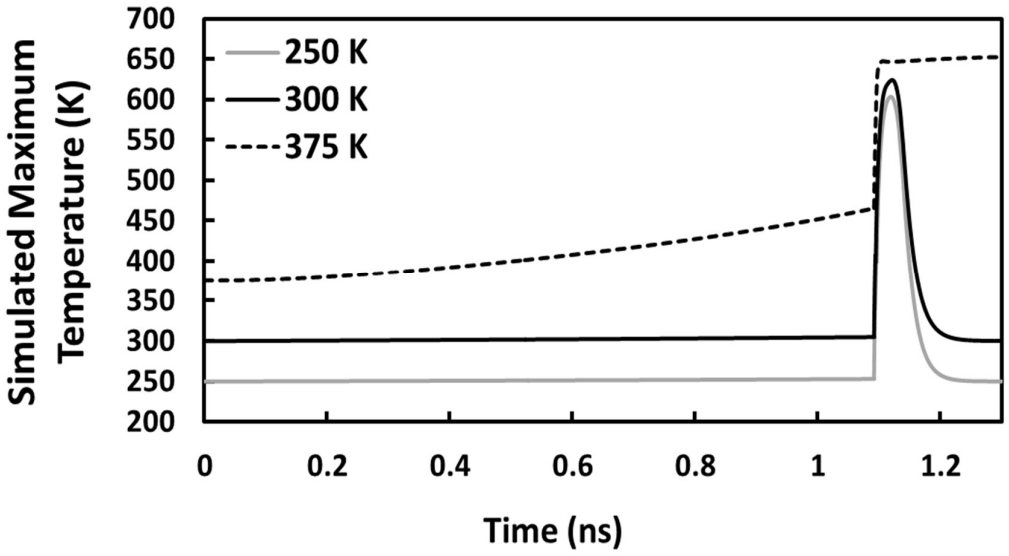


Figure 4.6-5 Simulated IGBT current during inductor charging and avalanche at different ambient temperatures.

Two-dimensional current density contour plots of the SiC MOSFET and silicon IGBT were also extracted from the finite element simulator. The results are shown in Figure 4.6-6 for the MOSFET and Figure 4.6-7 for the IGBT. In the case of the MOSFET the current flow is

concentrated, whereas in the IGBT the current flow is dispersed. This is likely due to the fact that the voltage blocking drift layer of the SiC MOSFET is much thinner than that of the IGBT as a result of the higher critical electric field in SiC. The lower value of the thermal time constant of SiC means that heat is dissipated faster than that of silicon; hence, the temperature surge does not initiate bipolar latch-up as is the case with the IGBT.

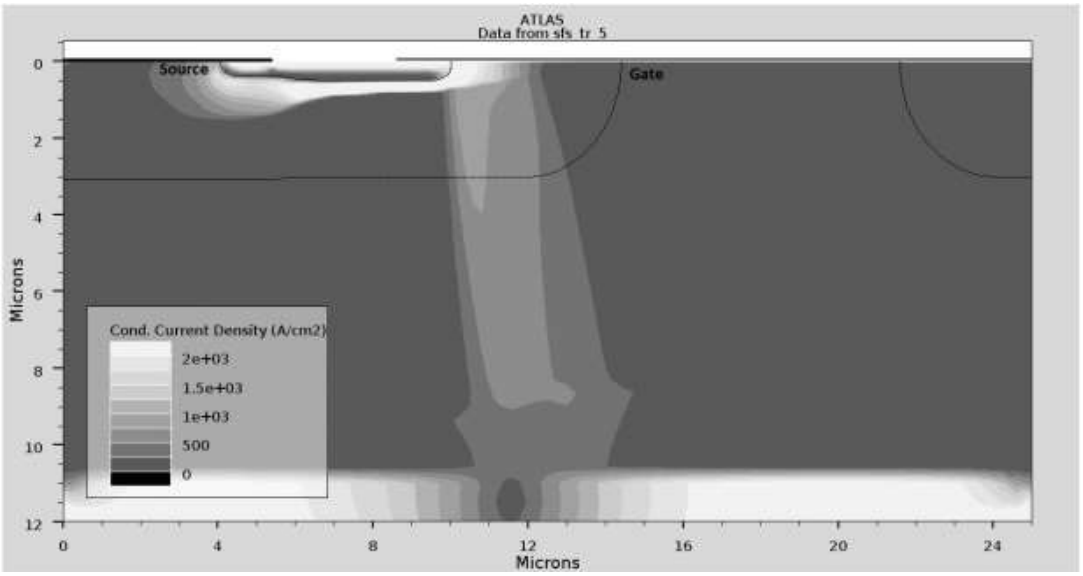


Figure 4.6-6 Two-dimensional current density plots for the SiC MOSFET

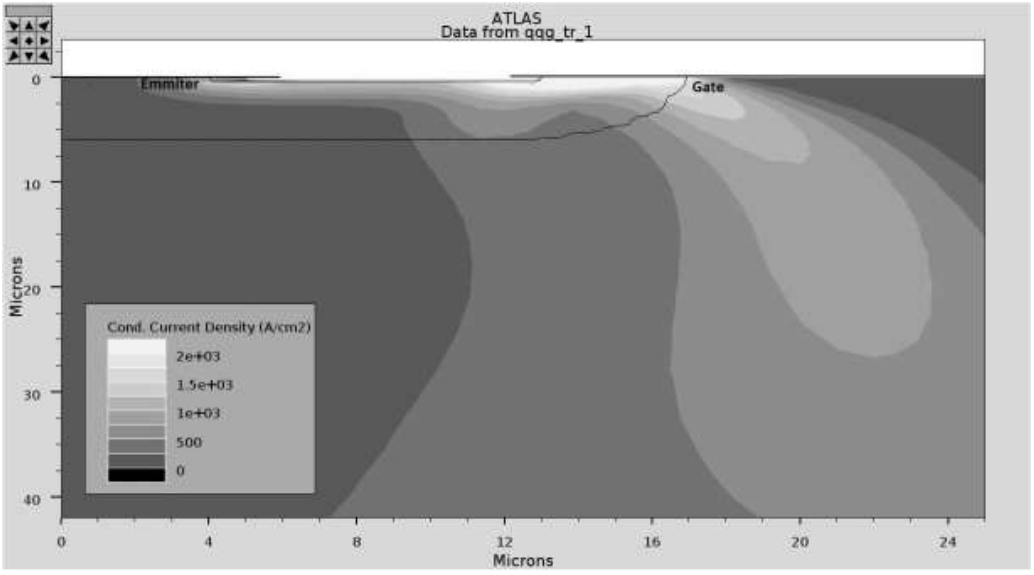


Figure 4.6-7 Two-dimensional current density plots for the silicon IGBT

4.7.Junction Temperature Calculation

Due to the nature of the test, it is very difficult to measure the junction temperature of the device using temperature sensitive electrical parameters during avalanche. However, the temperature can be calculated using electro-thermal equations that have been calibrated by finite element models. Using [58] it is possible to calculate the junction temperature when the device is in avalanche. The temperature is calculated using

$$T_J@n * \frac{t_{AV}}{10} = \begin{cases} \frac{P_O * K}{10} * \sqrt{\frac{t_{AV}}{10}} * \left[10 * \sqrt{n} - \sum_1^n \sqrt{n}\right], n \leq 10 \\ \frac{P_O * K}{10} * \sqrt{\frac{t_{AV}}{10}} * \left[10 * \sqrt{n} - \sum_{n-9}^n \sqrt{n}\right], n > 10 \end{cases} \quad (4.7\text{-}1)$$

Where T_J is the junction temperature, t_{AV} is the duration of the avalanche which is extrapolated from the measurements, P_O is the peak power also calculated from the measurements, K refers to the device thermal response and is calculated from the transient thermal impedance characteristic provided in the data sheet, n is the time step of the calculated temperature. The transient thermal characteristics for different ambient temperatures during avalanche for the SiC MOSFET are presented in Figure 4.7-1. The inductor used for the measurements in Figure 4.7-1 was 9.5 mH. Figure 4.7-2 shows the temperature transient characteristics for the SiC MOSFET during avalanche with different inductors (i.e. different avalanche durations). The ambient temperature used in the calculations of Figure 4.7-2 was 25˚C. Figure 4.7-3 and Figure 4.7-4 show similar calculated thermal transients for the silicon IGBT.

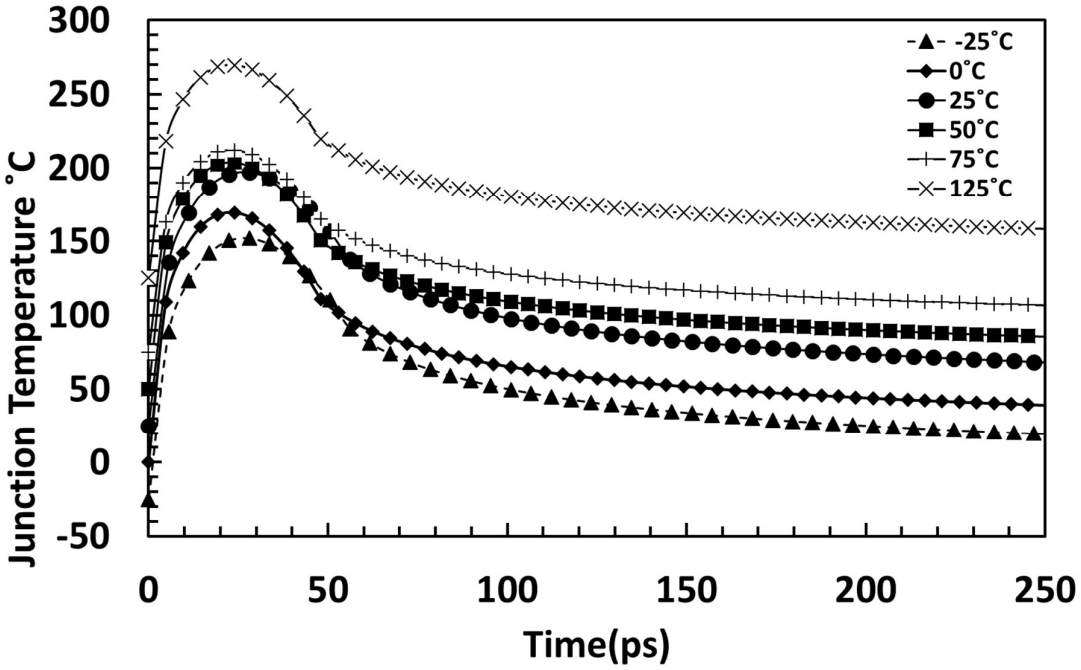


Figure 4.7-1 Junction Temperature for SiC MOSFET for different ambient temperatures

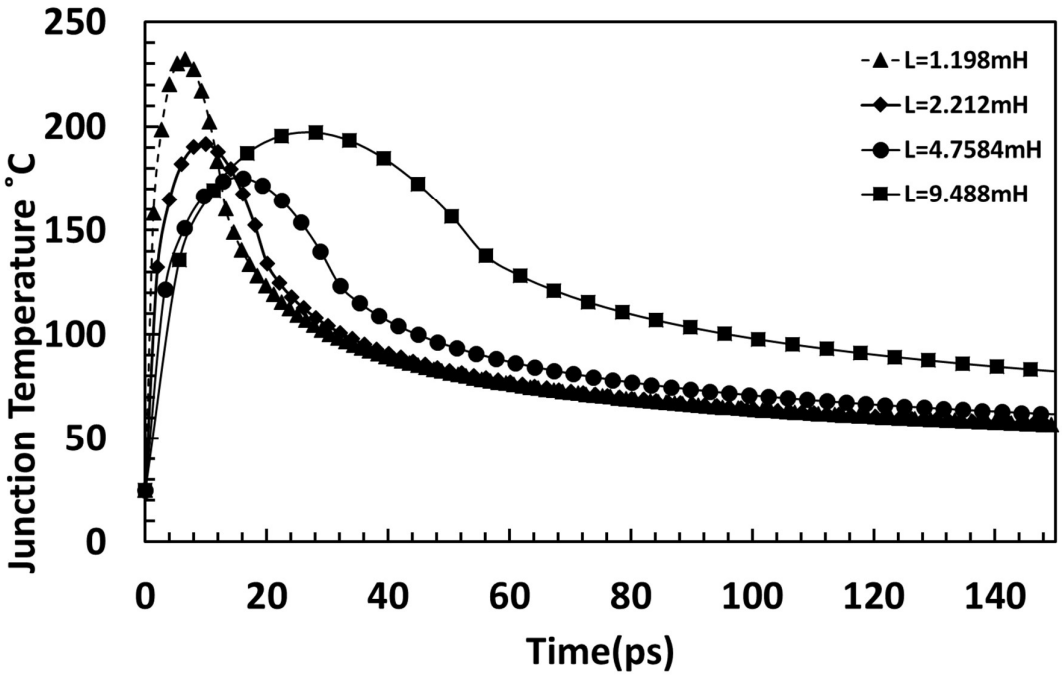


Figure 4.7-2 Junction Temperature for SiC MOSFET for different inductors

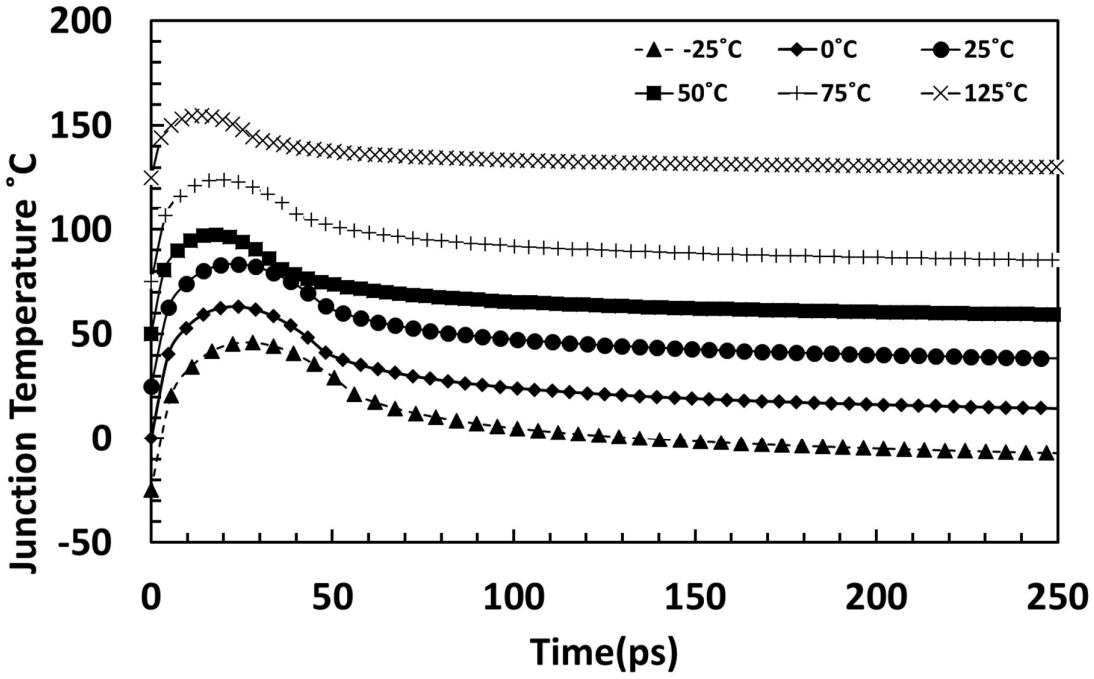


Figure 4.7-3 Junction Temperature for Si IGBT for different ambient temperatures

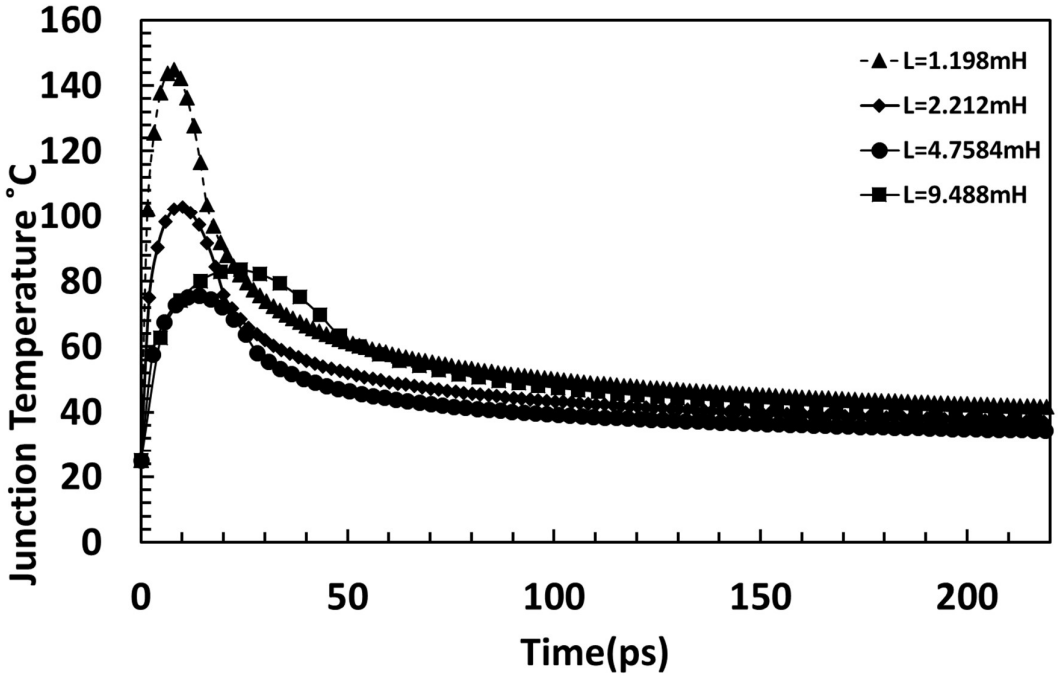


Figure 4.7-4 Junction Temperature for Si IGBT for different inductors

Figure 4.7-5 shows the peak calculated junction temperature for the SiC MOSFET and silicon IGBT at different ambient temperatures where a linear relationship can be observed. Figure 4.7-6 shows the peak junction temperature for both technologies with different inductors at 25 C.

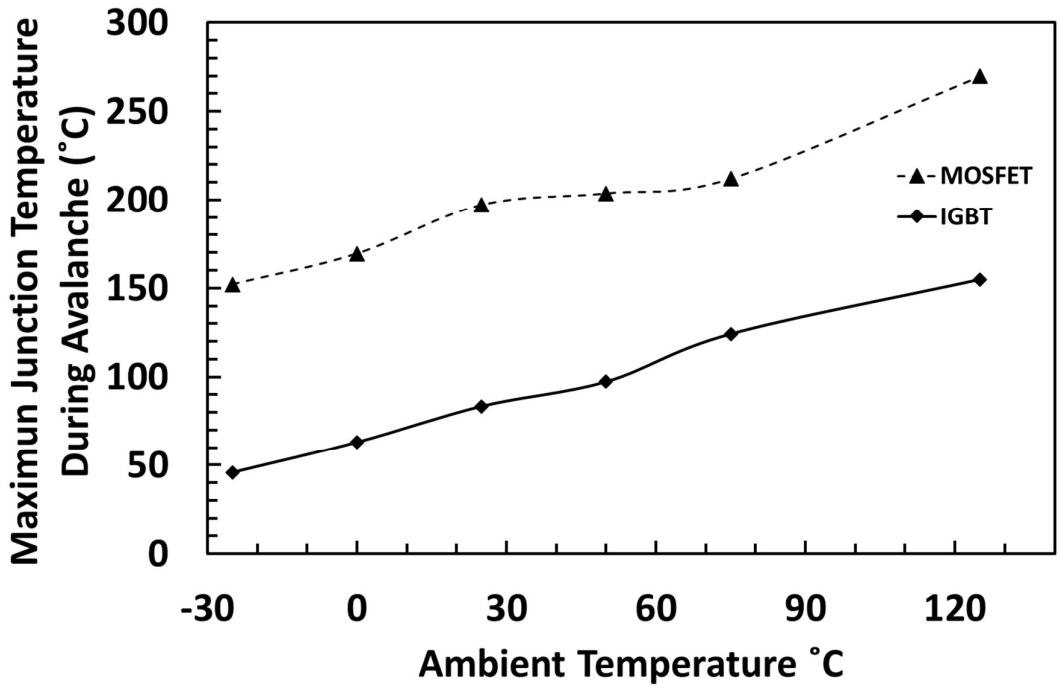


Figure 4.7-5 Comparison of peak junction temperatures for different ambient temperatures

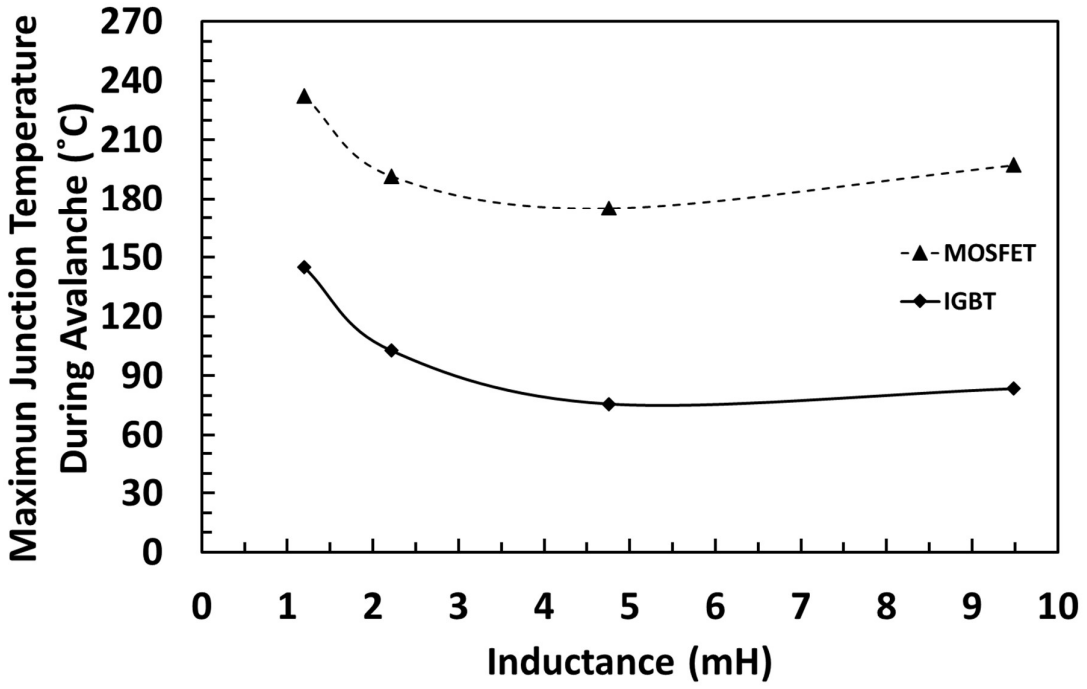


Figure 4.7-6 Comparison of peek junction temperatures for different inductances

Regardless that the junction temperature of the SiC MOSFET is higher than that of the Si IGBT the MOSFET is more resilient to avalanche. The thermal capabilities of SiC are the dominant factor for the avalanche capabilities of the device

4.8.Conclusions

In this chapter an avalanche description has been presented for both MOSFETs and IGBTs. The mechanism of how the parasitic BJT in a MOSFET and the parasitic thyristor in an IGBT turn on when the device is under avalanche mode conduction have also been presented. Power device failure in unclamped inductive switching can be triggered under two conditions namely, high avalanche current with a short avalanche duration (condition A) and a low avalanche current with a long avalanche duration (condition B). Under condition A, hot-spotting resulting from an unequal temperature distribution due to inter-cell parametric variation within the power device, is known to be the trigger mechanism. Whereas under condition B, the intrinsic semiconductor temperature limitation resulting from thermally induced bandgap narrowing is

thought to be the trigger mechanism. The experimental results have shown that SiC power MOSFETs are shown to be more avalanche rugged under condition B for the same avalanche energy compared to condition A. In the case of IGBTs, there is not a significant difference between the two conditions as far as the maximum avalanche energy is concerned. UIS tests have also been performed when the DUT is used to pre-charge the inductor (condition C) and when another device is used to pre-charge the inductor while the gate of the DUT is clamped to its source (condition D). SiC power MOSFETs are shown to be significantly more rugged in condition D compared to condition C. The results show that the material property of the semiconductor is more critical for determining avalanche mode ruggedness than the device type.

Also the mechanism of parasitic bipolar latch-up during avalanche mode conduction has been investigated for 1.2 kV/25 A SiC MOSFETs and 1.2kV/30A silicon IGBTs. It has been shown that the SiC MOSFET is more electrothermally rugged and can withstand higher temperature surges in spite of the fact that it has a lower current rating. The SiC device can withstand avalanche current 40% greater than the rated current at lower temperatures but not at higher temperatures. The IGBT is unable to withstand avalanche currents 16% beyond its rating. The SiC MOSFET can also withstand avalanche currents at the rated value at 125 °C.

An electrothermal model was developed that explained why elevated temperatures accelerate the latching of the parasitic BJT and the results are confirmed by finite element modelling, the model was described in chapter 2. The experimentally extracted maximum operation temperatures (extracted from avalanche current vs. temperature plots) were compared with theoretical calculations using the temperature dependence of the intrinsic carrier concentration. The results showed a difference probably due to packaging constraints and process imperfections and that the SiC device is capable of withstanding approximately 3 times the temperature of Si. This was also supported by the finite element models.

5. Repetitive avalanche testing

5.1. Introduction

There have been some investigations into the repetitive avalanche capability of SiC power MOSFETs. Repetitive avalanche is simply when avalanche pulses within the reverse bias safe-operating-area of the device are repetitively passed through the device. As opposed to single avalanche stress tests, this is a thermos-mechanical test as well as an electrothermal test. Similar to power cycling tests, the junction temperature of the MOSFET is subjected to repetitive temperature excursions which impose certain mechanical stresses on the critical interfaces of the device. These critical interfaces include the source wire to top-metal interface as well as the semiconductor die to solder/substrate interfaces. However, repetitive avalanche tests are different from power cycling tests because of the significantly higher temperatures involved. In power cycling tests, a DC current pulse is switched ON and OFF through the device hence, the drain voltage is never raised. However, in repetitive avalanche tests, an inductor forces a current through an OFF state device resulting in simultaneously high currents and voltages. Furthermore, the drain voltage during avalanche mode conduction is the actual breakdown voltage of the MOSFET which is typically 30% higher than its rated voltage. For example, a 1.2 kV SiC MOSFET conducting a peak avalanche current of 10 A will be subjected to an instantaneous power of 15 kW over several microseconds depending on the size of the inductor.

A number of 1.2 kV SiC MOSFTs have been subjected to hundreds of thousands of avalanche pulses. 1.2 kV silicon power MOSFETs have also been tested in order to determine the impact of the wide bandgap material on the performance of the device under repetitive avalanche. The electrical parameters of the device, including the threshold voltage and transconductance, were measured at defined intervals during the avalanche pulses. The change

in the electrical parameters have been compared for both SiC and silicon power MOSFETs and the role of drain-avalanche induced hot carrier injection has been assessed for both devices. Furthermore, by varying the duration of the cooling period during the repetitive avalanche pulses, the average junction temperature has been varied for both devices. Hence, the impact of the junction temperature on drain avalanche induced HCI is assessed.

5.2. Repetitive avalanche Experimental results

The devices that were analyzed were, a SiC MOSFET from CREE with datasheet reference CMF10120D and an IXYS silicon MOSFET (IXFX20N120P). The test rig comprises of a power supply, DC link capacitor, inductor, gate-drive and the DUT.

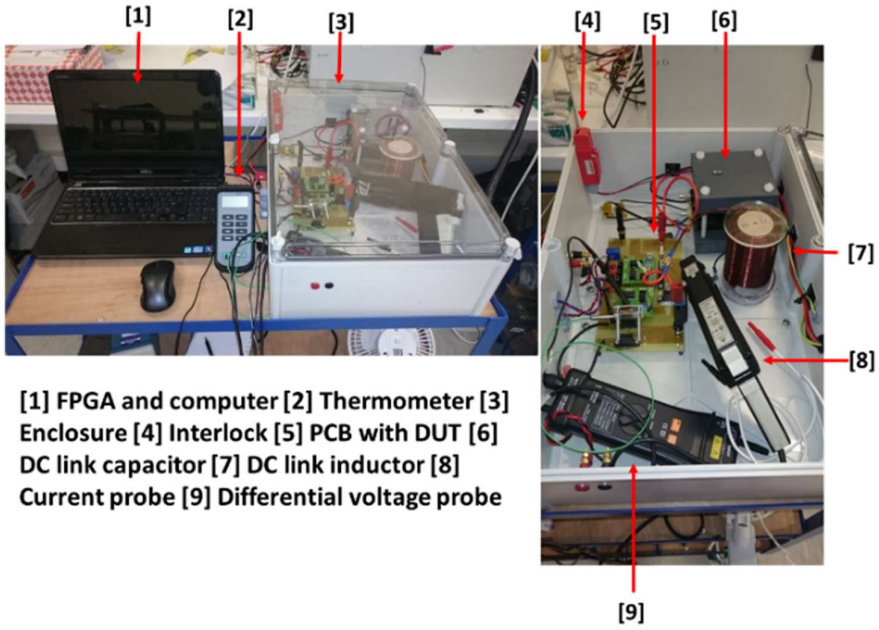


Figure 5.2-1 Repetitive avalanche experimental set up

The circuit diagram is the same as the single pulse test. The experiment is set in a way that before each test the DUT is not damaged and each of the pulses is captured in the oscilloscope. Also a counter measures the amount of cycles the device has endured. For this test the avalanche energy is significantly smaller than that of the single pulse testing. The scope of this test is to fatigue the devices in an electrothermal way and see which one can perform better.

The maximum avalanche current of the silicon and SiC power MOSFETs were determined for different avalanche durations at room temperature. This was done by varying the gate pulse duration (since the peak avalanche current is proportional to the gate pulse) for a given inductance and performing the UIS test until the device failed. It was observed that SiC power MOSFETs had a maximum current 10 times higher than the silicon MOSFET thus indicating that the wide bandgap nature of SiC makes it more electro-thermally rugged. The repetitive UIS tests were then performed by applying repetitive pulses within the RB-SOA for both devices. However, avalanche energy per pulse was 0.2 J for the SiC MOSFET and 3.5 mJ for the silicon MOSFET. The duration of the cooling period between each UIS pulse was used to set the average junction temperature for both devices. For the SiC MOSFET, a cooling period of 50 milliseconds resulted in an average case temperature of 127 °C and 40 milliseconds and case temperature of 152°C of whereas for the silicon MOSFET, a cooling period of 500 milliseconds resulted in an average case temperature of 81 °C.

Figure 5.2-2 shows the output characteristics (I_{DS} vs V_{DS}) of the SiC MOSFET at different intervals during the repetitive avalanche experiments. Figure 5.2-3 shows the transfer characteristics (I_{DS} vs. V_{GS}) for the same device at various intervals. It can be seen from both measurements that the on-state resistance degrades with increased avalanche cycling pulses. Figure 5.2-4 shows the output characteristics (I_{DS} vs V_{DS}) of the silicon MOSFET at different intervals during the repetitive avalanche experiments while Figure 5.2-5 shows the transfer characteristics (I_{DS} vs. V_{GS}) for the same device at various intervals. By comparing Figure 5.2-2 , Figure 5.2-3 and Figure 5.2-4, Figure 5.2-5, it is clear to see that the silicon MOSFETs degrade at a much faster rate compared to the SiC MOSFET in spite of having less energy per avalanche pulse and operating at a lower case temperature.

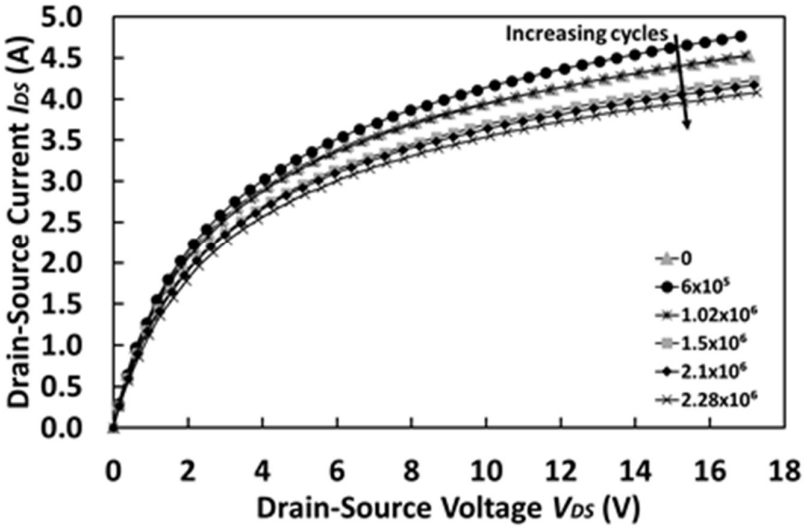


Figure 5.2-2 The output characteristics (I_{DS} vs V_{DS}) of the SiC MOSFET

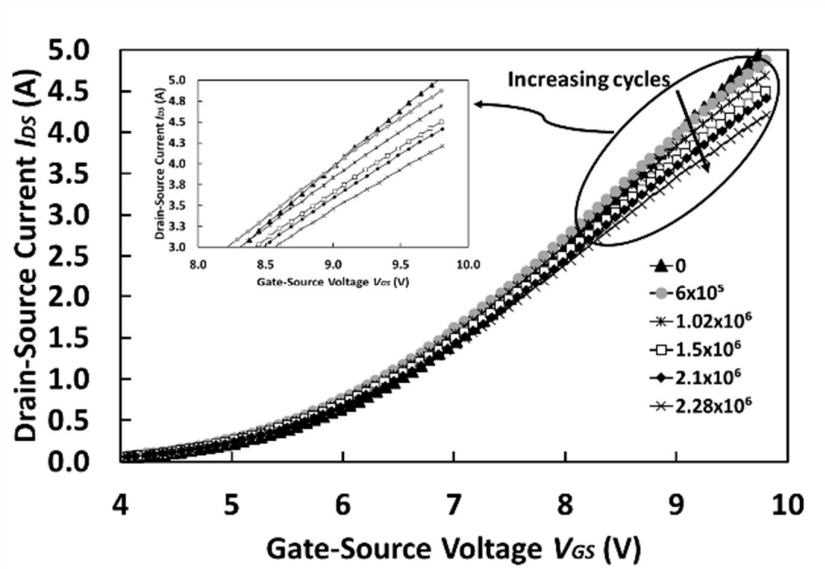


Figure 5.2-3 The corresponding gate transfer (I_{DS} vs V_{GS}) characteristics.

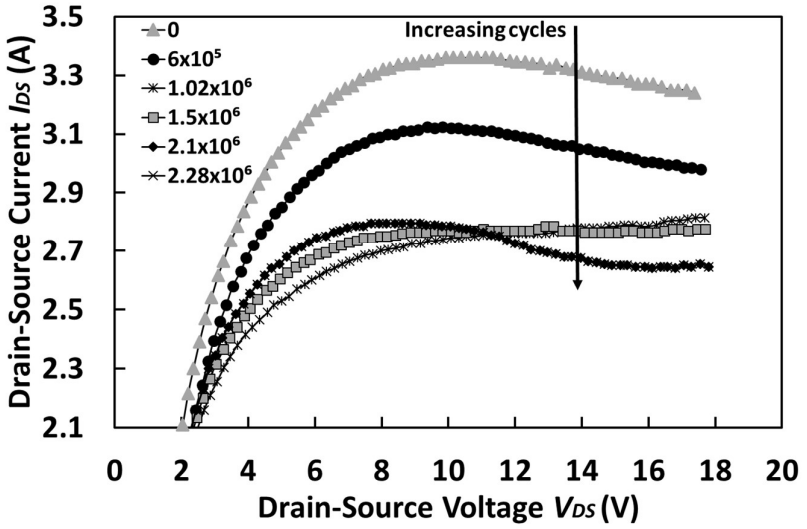


Figure 5.2-4 The output characteristics (I_{DS} vs V_{DS}) of the silicon MOSFET

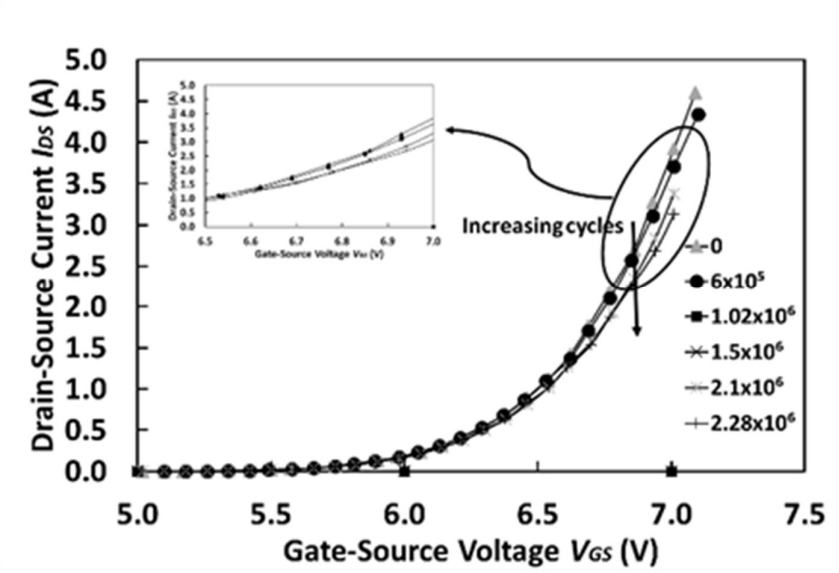


Figure 5.2-5 The corresponding gate transfer (I_{DS} vs V_{GS}) characteristics

Next the impact of the case temperature on the performance of the SiC MOSFET was investigated by varying the duration of the cooling period. By reducing the cooling period, the average case temperature is increased and vice versa. As the devices are tested under repetitive avalanche, the junction/case temperature increases up to the point where the rate of heat generation is equal to the rate of heat extraction. This point of thermal equilibrium will depend on the cooling period as well as the transient thermal impedance characteristics of the packaging system. Figure 5.2-6 shows the output (I_{DS} vs V_{GS}) characteristics for the SiC

MOSFET at different intervals during the repetitive avalanche tests for 2 different cooling durations corresponding to 2 different case/junction temperatures. Figure 5.2-7 shows a comparison of the normalized transconductance of the SiC MOSFETs as a function of the number of avalanche cycles. It can be seen that the rate of degradation of the transconductance is similar for the 2 temperatures although the transconductance reduces as the case temperature increases.

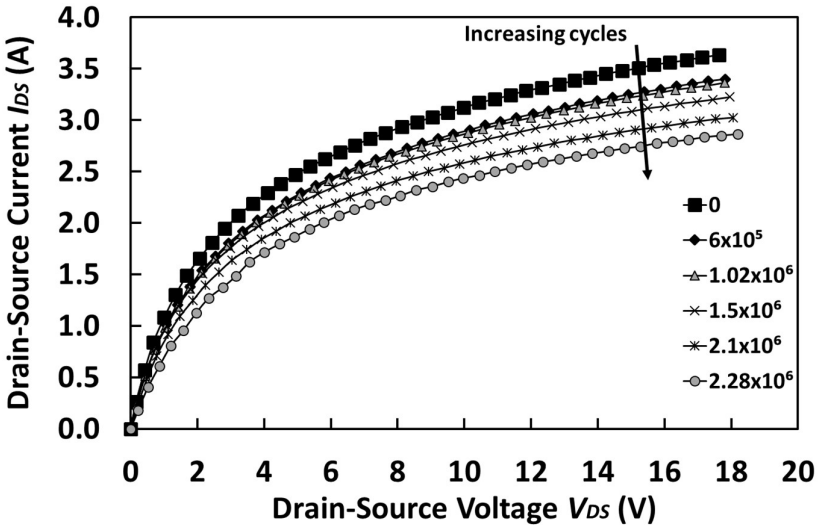


Figure 5.2-6 (I_{DS} vs V_{DS}) of the SiC MOSFET measured at different case temperatures

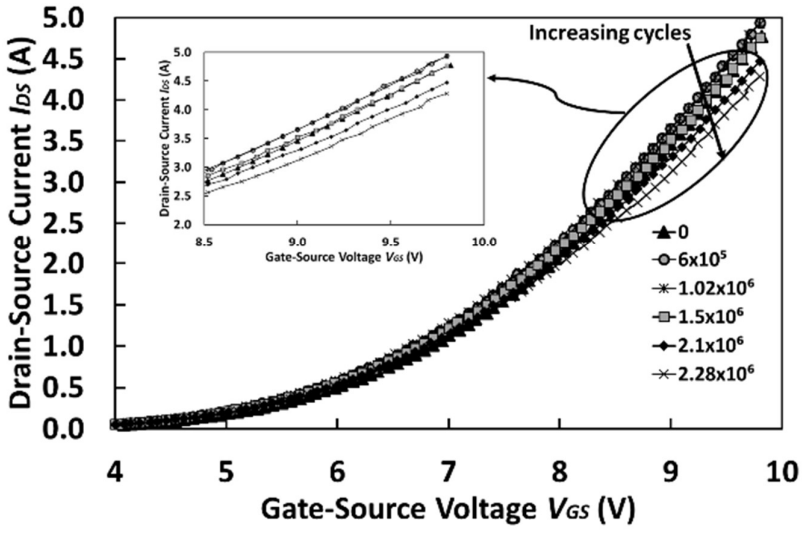


Figure 5.2-7 The transconductance of the SiC MOSFETs as a function of the number of cycles.

It is clear from the measurements presented previously that the rate of degradation of the transconductance in the silicon MOSFET is much higher than that in the SiC MOSFET. This is in spite of the fact that the average case temperature for the SiC MOSFET was 46.7% higher compared with the silicon and the avalanche energy per pulse was 98% higher than that of the silicon MOSFET. Figure 5.2-7 shows the maximum transconductance as a function of the number of avalanche cycles for both the SiC MOSFET and silicon MOSFET. It can be seen from Figure 5.2-8 that the rate of degradation in the maximum transconductance (which is quantified by the slope of the line of best fit is higher for the silicon MOSFET i.e. the magnitude of the slope is 0.96 for the silicon MOSFET and 0.15 for the SiC MOSFET. The maximum transconductance is higher for the silicon MOSFET because it is a much larger active area die and the case/junction temperature is 46% lower compared to the SiC MOSFET. Figure 5.2-9 shows the maximum transconductance as a function of the number of cycles for the SiC MOSFETs at different junction/case temperatures.

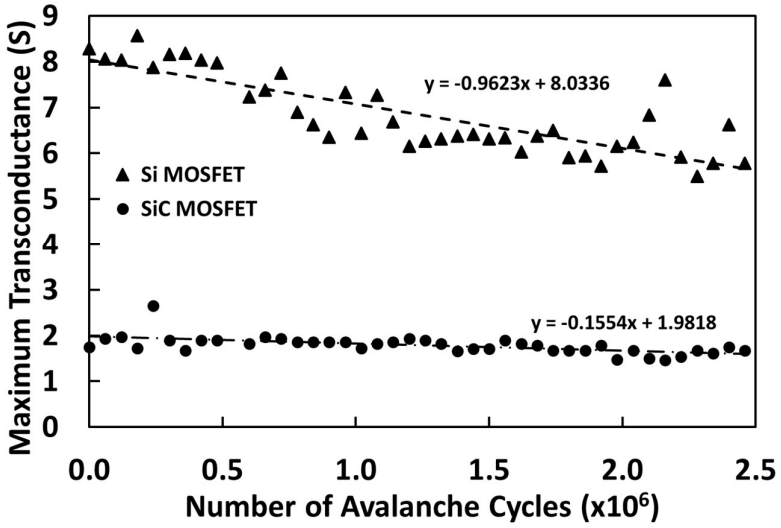


Figure 5.2-8 Comparison of transconductance between SiC device and Si Device

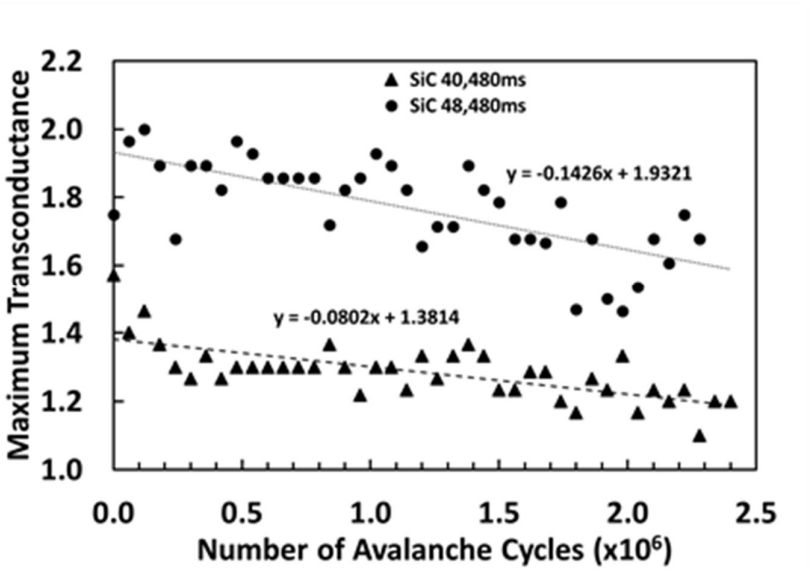


Figure 5.2-9 Comparison of transconductance between SiC devices at different avalanche durations

The degradation in the MOSFET's maximum transconductance is due to drain-avalanche induced hot carrier injection (DAI-HCI) as well as increased parasitic contact resistance between the wire-bond and the source metal. Avalanche mode conduction occurs via impact ionisation which involves electron-hole pair generation in the MOSFET. Hence, the generated electrons drift into the drain end of the MOSFET under the influence of the electric field while the holes are injected into the gate dielectric. This reduces the threshold voltage as well as the maximum transconductance by increasing carrier scattering.

A way of determining the intensity of the impact ionization is by calculating the impact ionization coefficient for the two materials (Si and SiC) at 25˚C. The impact ionization coefficient is simply defined as the number of electron-hole pairs generated by a carrier moving under the influence of an electric field [6]. As carrier collide with stationary atoms, they impart their kinetic energy into the atom and if this energy is greater than the bandgap of the semiconductor, an electron-hole pair is generated. Hence, since SiC has a greater bandgap than silicon, more energy is required for electron-hole pair generation, hence, SiC can block much higher voltages without undergoing avalanche breakdown compared to silicon. The equation for the impact ionization of electronics is given by

$$\alpha = ae^{-b/E} \qquad (5.2\text{-}1)$$

where E is the component of the electric field in the direction of current flow and & b are empirical parameters that depend on the semiconductor material and the temperature. For SiC,

$$a = 6.46 \times 10^6 - 1.07 \times 10^4 T \qquad \& \qquad b = 1.75 \times 10^7$$

Hence, at 25˚C, $a = 3{,}27 \times 10^6$ cm^{-1} and $b = 1.75 \times 10^7$V.cm^{-1}. For silicon at 25˚C, $a = 7 \times 10^5$ and $b = 1.23 \times 10^6$[6]. Hence, for a given electric field, the rate of impact ionization in the SiC MOSFET is significantly smaller than the silicon MOSFET. This implies that hot-carrier-injection resulting from the avalanche cycling will occur at a smaller rate in the SiC MOSFET compared to the silicon MOSFET. This explains why the maximum transconductance in the SiC MOSFET is less affected by the repetitive avalanche pulses.

6. Conclusions

Scope of this work is to investigate novel ways to model the switching behavior of wide bandgap semiconductor devices. Modelling the parasitics of these devices allows better control in high frequency switching applications and models that can run fast and reliably are of outmost importance. Using state space modelling allows to investigate the behavior of the devices in a fast way without significant loss in accuracy. State space modelling provides much better speed than finite element analysis but not the same accuracy. Investigating the behavior of the device and the effects the parasitic inductances and capacitances have on the device can also help avoid parasitic turn on of the devices as well as the effect of them on the device latching up during avalanche mode conduction.

Next a comparison between several devices was performed during avalanche mode conduction. The scope of that work was to investigate the differences between Si and Sic Devices as well as differences in architecture, differences between MOSFETs and IGBTs. Also avalanche mode conduction was used as new way of stressing the devices and determining which is the most rugged one. Finite element analysis was performed to validate the failure mechanisms of the devices. Mathematical models were also created and simulations were performed to validate the equations and the electrothermal instabilities in the devices. The results of these models were also validated form the finite element analysis. The tests were done altering as many variables as possible to determine which device performs better as well determining which is the major factor of device failure under these extremes conditions. The parameters investigated were energy, temperature, duration of conduction, ambient temperature etc. The results were very promising and present each effect any of these parameters have on the reliability of the device. Further work that can be done in this field is finding ways to detect the device degradation using avalanche mode conduction. Also further

work can be done using finite element analysis in conjunction with x-ray to see how the structure of the device is altered under avalanche. A similar type of test was conducted but repetitive avalanche testing was done at much lower energies to see the effect of this type of stress. SiC is a more robust device even in this type of tests. The reason being it's capabilities in high temperatures. In both single pulse vents as well as repetitive testing the week link for SiC MOSFETs is the packaging and probably the wire bonding. The material can withstand much larger temperatures compared to that of Silicon. The packaging technology used in this devices is the same as the IGBTs so the thermal limitations are the same. Companies have started using high temperature packaging for wide bandgap devices stating operating temperatures of 250ºC [59]. Sometimes avalanche conduction is the normal operation in certain applications. The absence of the diode makes the circuit much faster. This is very important in automotive applications where the need for fast solenoid discharging is paramount. Examples for this applications are the injector coil circuit and the Anti-locking Breaking System (ABS) pump which is connected directly to the battery. In Figure 5.2-10 and Figure 5.2-11 both of the applications are presented.[47, 60]

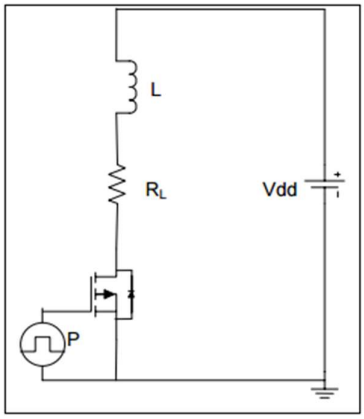


Figure 5.2-10 Automotive Injector Coil Circuit

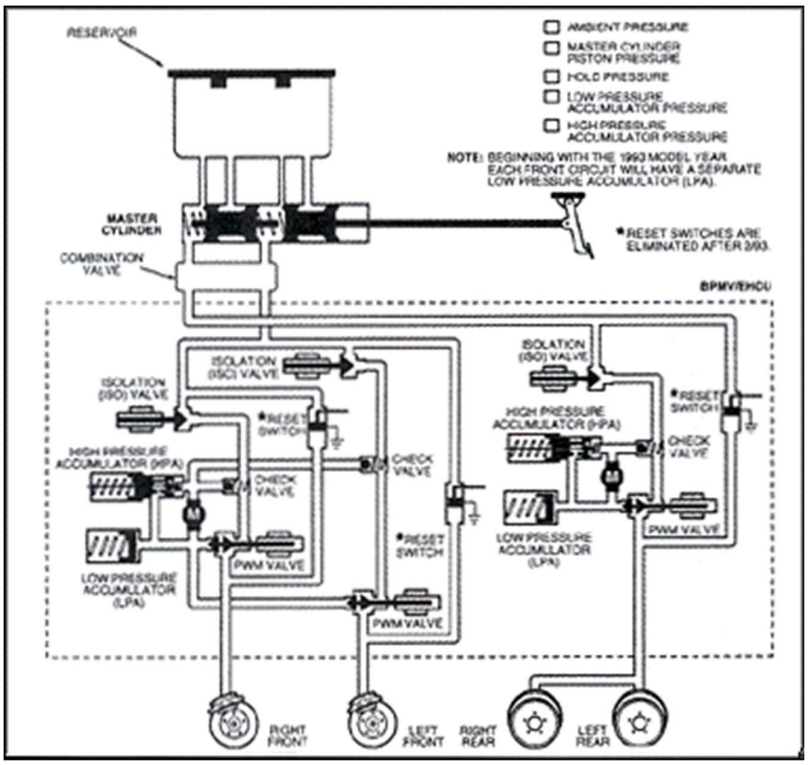


Figure 5.2-11 ABS system

Investigating novel ways of device modelling using more simple tools like MATLAB was one goals of this work. Also investigating different technologies under two different non-conventional mode conductions was investigated in conjunction with electrothermal modelling as well as trying to identify device degradation.

This work can be continued and further investigation can be performed in non-conventional device conduction. Applications in the automotive industry use this type of conduction to discharge inductive charges so reliability is paramount.

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8. Appendix

Modeling Power Converters using Hard Switched Silicon Carbide MOSFETs and Schottky Barrier Diodes

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Keywords

«MOSFET», «Parasitics», «Silicon Carbide (SiC)», «Simulation», «Switching losses»,

Abstract

The emergence of silicon carbide MOSFETs and Schottky Barrier Diodes (SBD) at higher voltage and current ratings is opening up new possibilities in the design of energy dense power converters. One of the main advantages of these wide bandgap unipolar devices is the use of fast switching to enable the size reduction of passive components. However, packaging constraints like parasitic inductances limit how fast the MOSFETs and diodes can switch, because of high frequency electromagnetic oscillations or ringing. Ringing is a reliability concern as it stresses the devices and causes additional losses to the switching losses. In this paper, a framework of power converter design is introduced based on the analytical modelling of current commutation between the MOSFET and the diode. The analysis of the model is done in the frequency domain which lends it to easy use and computational efficiency. The impact of the parasitic inductances on the switching transients have been analyzed. The models are compared with experimental measurements and are shown to provide fast and accurate analysis of the switching transients. The results show the necessity of accounting for ringing when modelling power losses.

Introduction

For many a decade now, the advantages of silicon carbide devices have been thoroughly publicised and recorded. Power converters implemented in SiC MOSFETs and Schottky diodes have been demonstrated and compared with identical modules in Silicon IGBTs and PiN diodes with a 40% improvement in energy density. As a semiconductor material, the advantages of SiC over silicon are very well known. The higher critical field enables lower conduction losses for a given breakdown voltage rating and the higher thermal conductivity makes it more suitable for harsh operating environments. Furthermore, the improved energy density in SiC means lower terminal parasitic capacitances which is crucial for faster switching. Another benefit of fast switching unipolar SiC technology is its enablement of size reduction of passive components, which is vital in applications where weight and volume come at a premium.

However, the fast switching output transients (dI_{DS}/dt and dV_{DS}/dt) coupled with parasitic capacitances and inductances from the package or module, cause electromagnetic instability in the form of ringing. This is a reliability concern from the point of view of increased losses and electromagnetic interference. Furthermore, excessive ringing may take the device beyond its rated capacity. Hence, it is important to be able to accurately model and characterize the additional power losses and terminal instability that arise from fast switching transients in the presence of parasitics. Early MOSFET and diode switching models did not take into account the parasitic inductances, hence could not distinguish the ringing from fast switching. Subsequent models took into consideration the source and drain inductances and were implemented in the time domain, which yielded mathematical expressions that do not lend easy use. In the model developed in [1], the gate, source and drain inductances have been taken into account. However, because the model was developed for low voltage MOSFETs with shorter switching transients, the effects of the parasitic elements are less pronounced. Also the switching waveforms do not show any oscillations, therefore ringing losses are not considered. As the switching frequency is increased with higher voltage/current ratings these cannot be neglected. In [2], switching transient analysis have been performed on a MOSFET with a free-wheeling diode and a snubber, however, there was no consideration of ringing or oscillations. Furthermore, the use of snubbers can counteract against the fast switching benefits that SiC unipolar devices deliver. In [3], the source and drain inductances have been taken into account as well as the non-linearity of the parasitic capacitors. In [4], the switching characteristics of SiC Schottky diodes are compared with silicon PiN diodes and it is shown that ringing occurs for the SiC diode and can contribute to the total switching losses.

In this paper, the switching characteristics of SiC MOSFETs and SiC Schottky diodes have been modelled and experimentally characterized for different gate resistors. All parasitic elements -gate, source and drain inductances- have been considered and actual ringing has been modelled. The model accounts for current commutation between the diode and the MOSFET and analyses the impact of ringing on the power losses. The parasitic inductances and capacitances of the diode have also been incorporated. The model is developed and implemented in the frequency domain using MATLAB SIMULINK and is compared to experimental measurements of CREE SiC MOSFET (CMF20120D) and diodes rated at 1.2 kV. In section II the model is described; in section III experimental results are presented; in section IV the results are discussed and in section V the conclusions of the paper are presented.

Model Derivation

In this section of the paper the terminal voltage and current switching characteristics of the MOSFET and the diode are developed as a first principle. All parasitics including the gate (L_G), source (L_S) and drain inductances (L_D), as well as the gate-source (C_{GS}) and gate-drain (C_{GD}) capacitances are taken into consideration.

MOSFET Model

The classical gate charging characteristic shown in Fig. 1(a) are considered, where the gate voltage of a typical MOSFET is shown as a function of time. In Fig. 1(a), the gate-source voltage (V_{GS}) increases exponentially as the gate-source capacitor is charged between time t_0 and t_1. Between t_1 and t_2, the drain current (I_{DS}) increases and V_{GS} approaches the plateau voltage, which is when the gate-drain capacitance starts charging i.e. Miller effect. Between t_2 and t_3, the drain-source voltage (V_{DS}) collapses from the off-state blocking voltage to the on-state voltage which depends on the on-state resistance (R_{DSON}) and the forward current (I_{DS}). After C_{GD} has fully charged, V_{GS} resumes its exponential rise to the gate-drive voltage which is between time t_3 and t_4. Fig. 1(b) shows the experimental switching waveforms measured from 1200V/30A SiC MOSFETs (CMF20120D from CREE) where oscillations can be observed in the V_{DS}, V_{GS} and I_{DS} characteristics. Because the characteristics in Fig. 1(a) do not account for parasitic inductances, they are unable to capture oscillations in the device and will not be accurate in the calculation of switching losses or the prediction of ringing losses. To overcome this limitation and to more accurately model switching and

ringing losses, different techniques that take parasitic inductances into account have been presented. In [5, 6] SPICE was used for modelling the transients, in [7] SABER was used whereas in [8], time domain mathematical models were used. In this case, the MOSFET switching transients will be simulated for the different time frames i.e. V_{GS} changing (C_{GS} charging/discharging) and V_{DS} changing (C_{GD} charging/discharging).

From t_0 to t_1

Fig. 2 (a) shows the equivalent circuit of the MOSFET during this phase of switching when C_{GS} is charging and V_{GS} is below the threshold voltage. The following equations are derived by applying basic nodal analysis to the terminals of the MOSFET in the equivalent circuit

$$(V_D - V_G)sC_{GD} + \left(\frac{V_D - V_{DD}}{sL_D}\right) = 0 \quad (1)$$

$$(V_G - V_S)sC_{GS} + \left(\frac{V_G - V_{GG}}{R_G + sL_G}\right) + (V_G - V_D)sC_{GD} = 0 \quad (2)$$

$$(V_S - V_G)sC_{GS} + \frac{V_S}{sL_S} = 0 \quad (3)$$

V_{GS} is derived from these equations:

$$V_{GS} = \frac{As^2 - V_{DD} + V_{GG}}{A_1 s^4 + B_1 s^3 + C_1 s^2 + D_1 s + 1} \quad (4)$$

Where:

$$A = C_{GD} L_D V_{GG} - C_{GD} L_D V_{DD}$$
$$A_1 = C_{GD}C_{GS}L_G L_D + C_{GD}C_{GS}L_D L_S + C_{GD}C_{GS}L_G L_S$$
$$B_1 = C_{GS}C_{GD}L_G R_G + C_{GD}L_S C_{GS}R_G$$
$$C_1 = C_{GD}L_D + C_{GD}L_G + C_{GS}L_G + C_{GS}L_S$$
$$D_1 = C_{GD}R_G + C_{GS}R_G$$

From t_2 to t_3

The equivalent circuit for this phase of operation is shown in Fig. 2(b). During this time frame VGS is constant and VDS is changing due to the Miller effect. Using the same nodal analysis, the following equations are derived for VDS

$$(V_D - V_G)sC_{GD} + \left(\frac{V_D - V_{DD}}{sL_D}\right) + \left(\frac{V_D - V_S}{R_{DSON}}\right) = 0 \quad (5)$$

$$(V_G - V_S)sC_{GS} + \left(\frac{V_G - V_{GG}}{R_G + sL_G}\right) + (V_G - V_D)sC_{GD} = 0 \quad (6)$$

$$(V_S - V_G)sC_{GS} + \left(\frac{V_S - V_D}{R_{DSON}}\right) + \frac{V_S}{sL_S} = 0 \quad (7)$$

V_{DS} is derived from these equations:

$$V_{DS} = \frac{K}{(sR_G C_{GD} + 1)} \frac{A_2 s^2 + B_2 s + R_{DSON} V_{DD}}{A_3 s^4 + B_3 s^3 + C_3 s^2 + D_3 s + R_{DSON}} \quad (8)$$

Where:

$$A_2 = C_{GD}L_G R_{DSON}V_{DD} + C_{GD}L_D R_{DSON}V_{GG} + C_{GS}L_G R_{DSON}V_{DD} + C_{GS}L_S R_{DSON}V_{DD} - C_{GS}L_S R_{DSON}V_{GG}$$
$$B_2 = C_{GD}R_{DSON}R_G V_{DD} + C_{GS}R_G R_{DSON}V_{DD}$$
$$A_3 = C_{GD}C_{GS}L_G R_{DSON}L_S + C_{GD}C_{GS}L_G L_S R_{DSON}$$
$$B_3 = C_{GD}L_G L_D + C_{GS}L_D L_G + C_{GD}L_G L_S + C_{GS}L_D L_S + C_{GD}L_G L_S + C_{GS}L_G L_S + C_{GD}C_{GS}L_D R_{DSON}R_G + C_{GD}C_{GS}L_S R_{DSON}R_G$$

$$C_3 = C_{GD}L_D R_{DSON} + C_{GD}L_D R_G + C_{GS}L_D R_G + C_{GD}L_G R_{DSON} + C_{GS}L_G R_{DSON} + C_{GS}L_S R_{DSON} + C_{GD}L_S R_G + C_{GS}L_S R_G$$

$$D_3 = L_D + L_S + C_{GD}R_{DSON}R_G + C_{GS}R_{DSON}R_G$$

DIODE model

Similar principles have been adopted for modelling the transient characteristics of the diode. The diode can be modelled as a stray inductance, voltage dependent depletion capacitance and a parasitic series resistance as shown in Fig. 3(a) and (b) [4]. The equation for the diode transients can be developed from the transfer function of the diode equivalent circuit and the input voltage

$$V_{AK} = \frac{V_{DD}}{(sR_G C_{GD}+1)} \frac{\frac{R_S+R_{AK}}{R_{AK}L_{stray}C_{AK}}}{s^2+\left(\frac{R_S R_{AK}C_{AK}+L_{stray}}{R_{AK}L_{stray}C_{AK}}\right)s+\frac{R_S+R_{AK}}{R_{AK}L_{stray}C_{AK}}} \quad (9)$$

The transfer function of the diode equivalent circuit is also used to model the electrical current commutation between the diode and the MOSFET the difference is the value used for RS. The results of the model will be compared with experimental measurements.

Experimental results

The experimental set-up can be seen in Fig.4 (a). The devices used were CREE's SiC 1200 V/33 A MOSFET and the diode was an Infineon 200 A SiC diode. The circuitry consists of a half bridge with two MOSFETS in parallel and one diode. The freewheeling diode was connected across an 800 µH inductor. The supply voltage (VDD) was set to 200 V and the gate drive voltage (VGG) was set to 18V. The gate was connected to a Tektronix AFFG3022 signal generator through an optocoupler (HCPL 3120) for protecting the pulse generator from any power surges. The results were taken from a Tektronix TDS5054 digital oscilloscope and the static characteristics of the devices were measured by a Tektronix curve tracer. The current through the device was measured with the digital oscilloscope through a Tektronix TCP303 current probe.

Results and discussion

As the MOSFET switches ON, V_{GS} rises from zero to the gate-drive voltage (V_{GG}) and V_{DS} falls from the supply voltage (V_{DD}) to the on-state voltage. Also, the free-wheeling diode voltage (V_{AK}) rises from the on-state voltage drop to V_{DD}. The current, initially free-wheeling through the diode starts diverting into the MOSFET. Fig. 5(a) compares the experimentally measured V_{GS} turn-ON transient with the simulated transient when switched with a gate resistance (R_G) of 22 Ω. Fig. 5(b) shows the same comparison when switched with an R_G of 100 Ω. To obtain similar characteristics, values of the parasitic inductances have been varied typically between tens of nH and a few µH. The diode and MOSFET parasitic inductances (L_G, L_S, L_D and L_{stray}) affecting the measurements not only result from the stray packaging and module inductances but also due to the actual measurement set-up. Average values of C_{GD} and C_{GS} were taken from the device datasheets since these capacitances are voltage dependent and hence, are not constant during the switching transient. It can be seen in Fig. 5 that increasing the gate resistance increases the duration of the gate-turn-ON transient and also dampens the oscillations on V_{GS}.

Fig. 6 shows the modelled and measured V_{DS} transient during MOSFET turn-ON for R_G = 22 Ω in 6(a) and 100 Ω in 6(b). In Fig. 6 as in Fig. 5, a good matching is observed between the measured and the modelled characteristics over the two gate resistances, with the 100 Ω measurements showing a longer transient. Although the model sufficiently predicts ripples in the V_{DS} turn-ON transient, the variations between the modelled and measured turn on transients are due to the fact that dynamic capacitances are not used in the model. The V_{DS} transient occurs during the discharge of C_{GD}, hence, the model can be further improved if a computationally efficient way of accounting for dynamic capacitances were developed. Fig. 7 shows the impact of the source inductance on the V_{DS} transients. It can be seen that

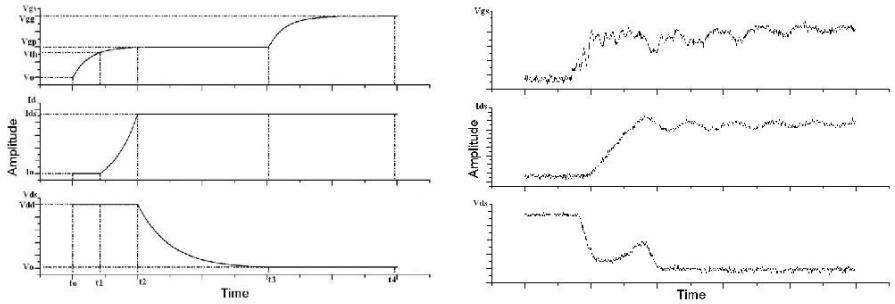
larger source inductances increase the amplitude of the V_{DS} oscillations during turn ON. This will also impact the magnitude of the peak voltage over-shoot during turnOFF.
Fig. 8(a) shows a comparison of the modelled and measured diode voltage (V_{AK}) transients during turn-ON for R_G=22 Ω whereas Fig. 8(b) shows the diode current (I_{AK}) transients. A good matching is observed in both of them. Fig. 9 shows the measured and modelled V_{AK} and I_{AK} transients for R_G=100 Ω where it can be seen that the peak overshoot and the amplitude of the V_{AK} is reduced. The models from (1) to (9) emulate very accurately the experimental measurements as can be noticed in Fig. 5 to 9.

Switching Losses

The models developed can be used to estimate the switching losses of hard switched SiC MOSFETs and diodes. In Fig. 10, the losses of the MOSFET are presented for both the 22 and 100 Ω gate resistances. It is evident from Fig. 10 that the power losses are higher for R_G = 100 Ω as expected because of the longer switching duration. The energy dissipated by the MOSFET when switched with an R_G of 22 Ω is 469.32 mJ for the model and 552.5 mJ for the measurements yielding an error of 15%. For R_G = 100 Ω the model calculates losses of 2457.5 mJ whereas the experimental measurements exhibit 2148.8 mJ yielding an error of 12.56%. The measured and modelled results for the diode losses are presented in Fig. 11 for the 22 and 100 Ω gate resistance switching. Similar to the MOSFET losses, the diode switching losses increase when R_G goes from 22 Ω to 100 Ω. The losses for the diode when switched with R_G= 22 Ω are 879.3 mJ for the model and 763.1 mJ for the experimental measurements yielding an error of 13%. When switched with R_G = 100 Ω, the model calculates 1135 mJ and the measurements exhibit 1063.3 mJ thereby yielding an error of 6.35%. Unlike the MOSFET, the diode shows significant ringing losses in the form of additional power spikes beside the main switching power spike. These ringing losses are larger for the device when switched at a 22 Ω gate resistance as a result of the faster switching i.e. larger dI_{DS}/dt. For the MOSFETs, the total measured switching energy losses increases by 74.3% when R_G is increased from 22 Ω to 100 Ω whereas for diodes the power loss increases by 28.2%.

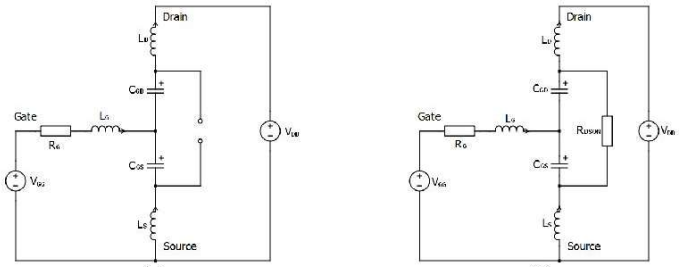
Conclusions

The turn-ON dynamic characteristics of a SiC MOSFET as well as a Schottky SiC diode have been modelled accurately using a new computationally efficient frequency domain technique. The model includes the impact of parasitic inductances. The results show that accounting for parasitic inductances is necessary for correctly simulating the switching and ringing losses. Increasing the gate resistance reduces the ringing losses although at the expense of increasing the switching losses which increase with the gate resistance due to longer transients. Adding a dynamic aspect to the values of the stray capacitors will make the model more precise making the fitting even better. This modelling technique can be used to improve module and packaging design because it enables an accurate assessment of the impact of parasitic inductances.



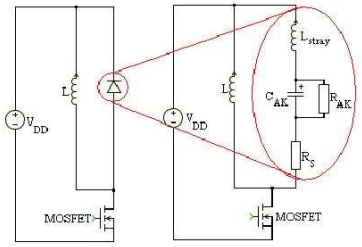
(a) (b)

Fig.1. (a) Ideal turn-on characteristics for V_{GS}, I_D and V_{DS} respectively (b) Measured turn-on graphs for V_{GS}, I_D and V_{DS} respectively



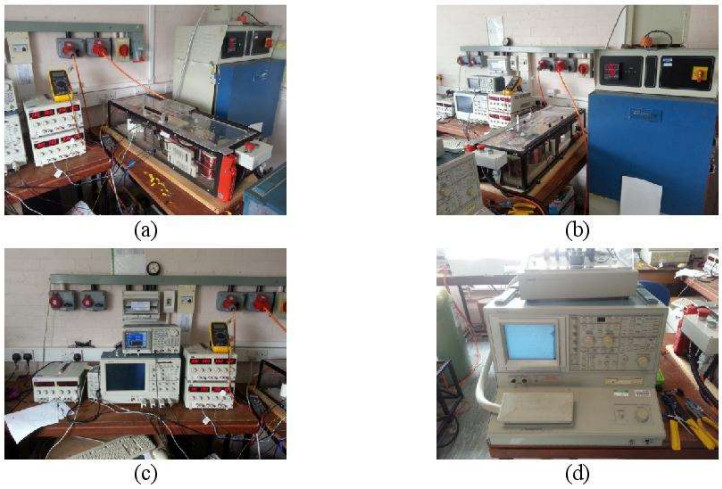
(a) (b)

Fig 2. Equivalent circuits for the MOSFET (a) from t_0 to t_1 and (b) from t_2 to t_4



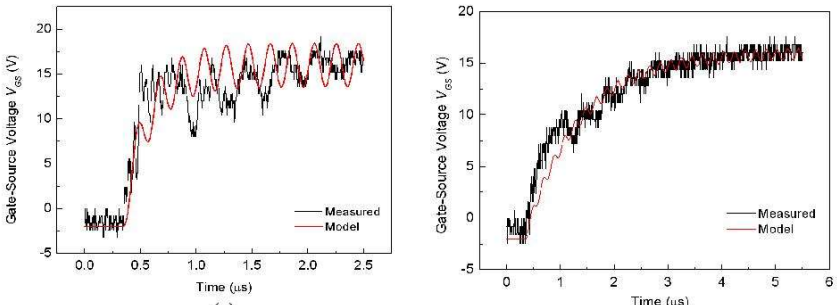
(a) (b)

Fig 3. (a) Clamped inductive switching test rig (b) Equivalent circuit showing the diode parasitics



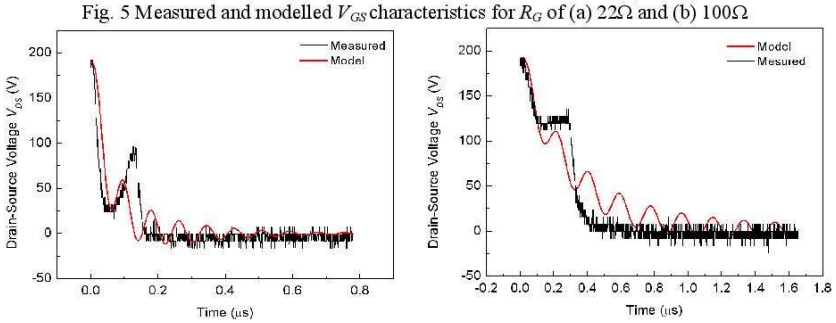
(a) (b) (c) (d)

Fig. 4.(a),(b) Experimental test rig and environmental chamber, (c) Measuring equipment, (d) Tektronix curve tracer



(a) (b)

Fig. 5 Measured and modelled V_{GS} characteristics for R_G of (a) 22Ω and (b) 100Ω



(a) (b)

Fig. 6 Experimental and modelled V_{DS} for a gate resistance of (a) 22 Ω and (b) 100 Ω

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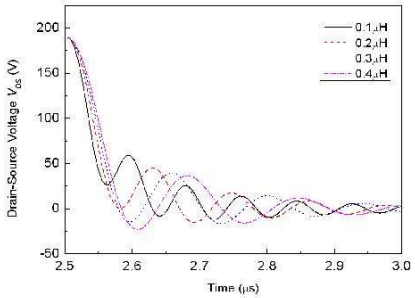
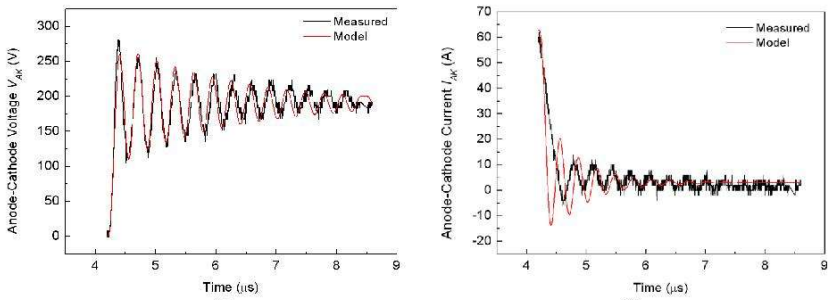
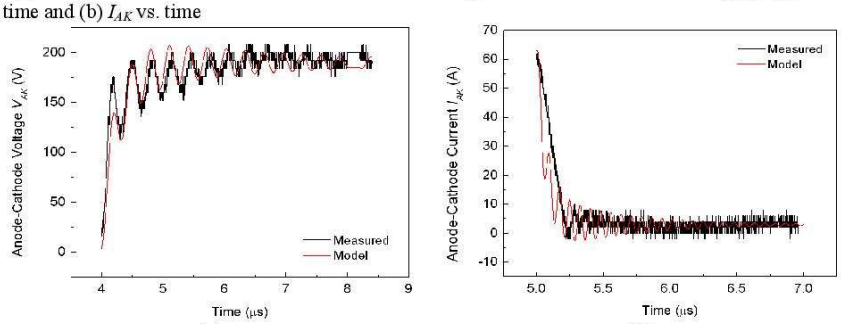


Fig.7 V_{DS} transient characteristics for different values of L_S



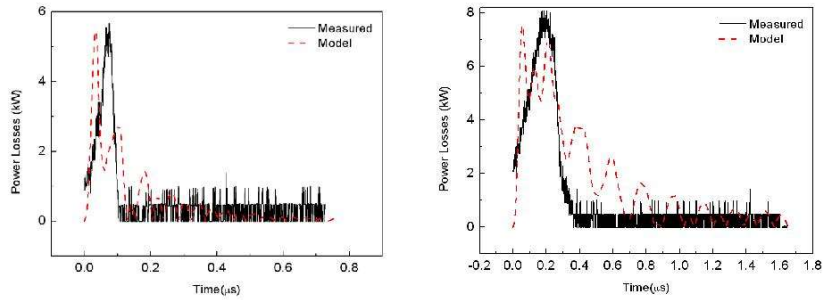
(a) (b)

Fig. 8. Experimental and modelled diode transients for a gate resistance of 22 Ω showing (a) V_{AK} vs. time and (b) I_{AK} vs. time



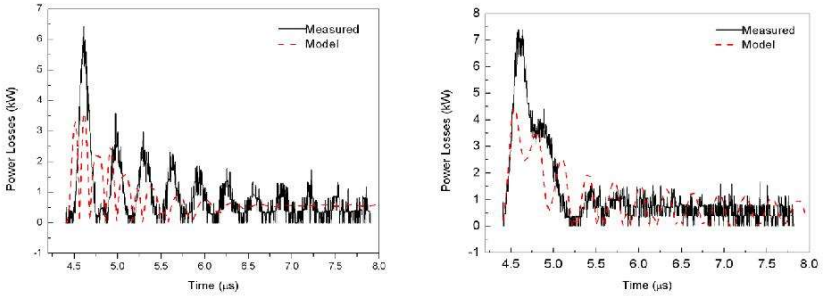
(a) (b)

Fig. 9. Experimental and modelled diode transient characteristics for a gate resistance of 100 Ω showing (a) V_{AK} vs. time and (b) I_{AK} vs. time



(a) (b)

Fig. 10. MOSFET losses for (a) 22Ω gate resistance and (b) for 100Ω gate resistance



(a) (b)

Fig. 11. Diode losses for (a) 22Ω gate resistance and (b) for 100Ω gate resistance

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Improved Electrothermal Ruggedness in SiC MOSFETs Compared With Silicon IGBTs

Petros Alexakis, Olayiwola Alatise, Ji Hu, Saeed Jahdi, Li Ran, and Philip A. Mawby

***Abstract*— A 1.2-kV/24-A SiC-MOSFET and a 1.2-kV/30-A Si-Insulated gate bipolar transistor (IGBT) have been electrothermally stressed in unclamped inductive switching conditions at different ambient temperatures ranging from −25 °C to 125 °C. The devices have been stressed with avalanche currents at their rated currents and 40% higher. The activation of the parasitic bipolar junction transistor (BJT) during avalanche mode conduction results from the increased body resistance causing a voltage drop between the source and body, greater than the emitter–base voltage of the parasitic BJT. Because the BJT current and temperature relate through a positive feedback mechanism, thermal runaway results in the destruction of the device. It is shown that the avalanche power sustained before the destruction of the device increases as the ambient temperature decreases. SiC MOSFETs are shown to be able to withstand avalanche currents equal to the rated forward current at 25 °C, whereas IGBTs cannot sustain the same electrothermal stress. SiC MOSFETs are also shown to be capable of withstanding avalanche currents 40% above the rated forward current though only at reduced temperatures. An electrothermal model has been developed to explain the temperature dependency of the BJT latchup, and the results are supported by finite-element models.**

***Index Terms*— Ruggedness, SiC MOSFETs, unclamped inductive switching (UIS).**

I. Introduction

ELECTROTHERMAL ruggedness is an important reliability metric that quantifies the ability of the power semiconductor device to withstand electrothermal stresses. This electrothermal stress can result from the conduction under avalanche mode, where there is simultaneously high current flowing through the device and a high voltage across it. Some circuits purposely use MOSFETs in unclamped inductive switching (UIS) mode, but these are mainly automotive applications where the devices drive inductive loads without antiparallel free-wheeling diodes to commutate the current when the device is switched OFF [1]–[4]. Avalanche mode conduction can also be triggered by high *dV/dt* transients that coupled with parasitic capacitances can cause a body current to flow, thereby forward biasing the emitter–base junction of the parasitic bipolar junction transistor (BJT) [5]. The body current is usually generated by the charging of a depletion capacitance during voltage switching. MOSFETs can also suffer severe electrothermal stresses in forward mode conduction if biased in the linear mode (high-current and high-voltage conditions) [6]. It should be noted that linear mode bias refers to the saturation mode bias in MOSFETs ($V_{DS} > V_{GS} - V_{TH}$); however, because the condition was first considered for BJTs, the term linear mode (which for a MOSFET is the ohmic or triode region) has repeatedly been used for MOSFETs as well. Linear mode conduction can also occur during switching transients when the bias point of the device moves across the load line. However, since the electrical switching time constant is much smaller than the thermal time constant, it is less of a problem for reliable switch mode power MOSFETs.

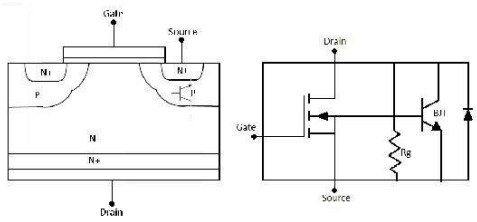

Fig. 1. MOSFET schematic diagram and equivalent circuit showing the antiparallel diode and n-p-n transistor.

All power MOSFETs, by virtue of their physical design, have antiparallel diodes as well as parasitic n-p-n BJTs. Ideally, the p-body of the MOSFET should be shorted to the source either by a high p-body implant dose away from the MOSFET channel (so as not to increase the threshold voltage excessively) [7] or by a moat structure with metal deposition shorting the n-source to the p-body. The purpose of shorting the body to the source is to ensure that there is no forward voltage drop between the body and the source. In reality, there is always some resistance between the source and the body, and this resistance will increase with temperature. Fig. 1 shows the schematic diagram of a vertical DMOSFET and the corresponding circuit model, showing the additional antiparallel diode and n-p-n parasitic BJT [8].

When current is flowing from the drain to the source through the channel, sufficient stray current flowing through the source-to-body resistance can cause the voltage drop across the source–body junction to forward bias the

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emitter–base junction of the parasitic BJT. The likelihood of this increases with temperature because of the positive temperature coefficient of the body resistance and the negative temperature coefficient of the in-built voltage across the source–body junction of the MOSFET (emitter–base junction of the parasitic BJT) [9]. Because BJT collector currents have a positive temperature coefficient, they are inherently unstable at high temperatures as a result of thermal runaway, i.e., a positive feedback process between current and temperature. In reality, power MOSFETs comprise numerous smaller FET cells sharing the same terminals. In ideal conditions, these smaller FET cells should share current equally. However, process-induced nonuniformities mean that there is always some current maldistribution. Therefore, process-induced electrical and thermal nonuniformities across the MOSFET cells will further enhance thermal runaway through current crowding. To mitigate this, UIS tests are usually done in the production line to screen out defective devices with process-induced nonuniformities that may compromise electrothermal ruggedness [5], [10].

In this paper, a 1.2-kV/24-A SiC MOSFET and a 1.2-kV/30-A silicon IGBT have been tested in UIS circuits at different temperatures. The devices have been tested to destruction at different ambient temperatures. Section II presents an electrothermal model that describes avalanche induced bipolar latchup. Section III describes the experimental setup as well as the results derived from the experiments. Section IV presents finite-element models of the devices, while Section V concludes this paper.

II. Electrothermal Model for Bipolar Latchup

An electrothermal model has been developed for the purpose of explaining the process of thermal runaway of MOSFETs conducting current in avalanche. The model uses an electrical input to calculate the temperature, which in turn is used to estimate temperature-dependent MOSFET parameters [11]. These MOSFET parameters (body voltage drop and in-built body potential) determine whether or not the parasitic bipolar has latched. The output is then fed back into the temperature model in a cyclical process. The model is based on an inductor forcing current through the MOSFET from the drain to the source, and assumes that the inductor has been precharged to a defined current. The current flowing through the MOSFET is described as

$$I_{(t)} = I_{\mathrm{AV}} - \frac{V_{(t)}t}{L} \tag{1}$$

where I_{AV} is the peak avalanche current, $I_{(t)}$ is the current flowing through the MOSFET, $V_{(t)}$ is the voltage across the MOSFET, L is the value of the inductor, and t is the time. The avalanche current is the peak current, and depends on how much current is initially stored in the magnetic field of the inductor. The inductance determines the peak value of the avalanche current together with the charging duration. The current determined from (1) is used to calculate the junction temperature of the MOSFET using

$$T_{(t)} = T_{\mathrm{AMB}} + R_{\mathrm{TH}} I_{(t)} V_{(t)} \left(1 - e^{-\frac{t}{R_{\mathrm{TH}} C_{\mathrm{TH}}}}\right) \tag{2}$$

where $T_{(t)}$ is the junction temperature of the MOSFET, T_{AMB} is the ambient temperature, R_{TH} is the thermal resistance of the MOSFET, and C_{TH} is the thermal capacitance of the MOSFET. The calculated junction temperature in (2) is used to calculate the built-in source to body p-n junction potential using [12]

$$\Phi_{\mathrm{bi}} = \frac{K_{\mathrm{B}} T_{(t)}}{q} \ln\left(\frac{N_{\mathrm{E}} N_{\mathrm{B}}}{n_{\mathrm{i}}^2}\right) \tag{3}$$

where Φ_{bi} is the built-in junction voltage of the parasitic BJT, K_{B} is the Boltzmann constant, q is the electric charge, N_{E} is the emitter (source) doping of the parasitic BJT (MOSFET), N_{B} is the base (body) doping of the parasitic BJT (MOSFET), and n_{i} is the intrinsic carrier concentration. The intrinsic carrier concentration has a temperature dependency that is material dependent and is different for silicon and SiC. Since SiC has a wider bandgap, it will have a lower intrinsic carrier concentration, and hence a higher built-in junction voltage (Φ_{bi}). For example, at 300 K SiC has an intrinsic carrier concentration of 1.5×10^{-8} cm^{-3}, whereas it is 1.5×10^{10} cm^{-3} for silicon. As a result, the built-in junction voltage for 4H–SiC will be approximately three times that of silicon [12]. As a consequence, the parasitic BJT will be harder to turn-ON in SiC since a greater voltage is needed to forward bias the emitter–base junction. The body resistance of the MOSFET is calculated using

$$R_{\mathrm{PB}} = \frac{l}{A N_{\mathrm{B}} q \mu_P} = \frac{l}{A N_{\mathrm{B}} q \cdot 495 \left(\frac{T}{300}\right)^{-2.2}} \tag{4}$$

where l is the length, A is the area, and μ_P is the hole mobility [12]. The voltage drop across the body resistance is calculated using

$$V_{\mathrm{PB}} = \frac{I_{\mathrm{C}}}{\beta} R_{\mathrm{PB}} \tag{5}$$

where I_{C} is the collector current of the parasitic BJT and β is the gain of the BJT. The condition for bipolar latchup is set by comparing V_{PB} to Φ_{bi}. The parasitic bipolar latches when $V_{\mathrm{PB}} > \Phi_{\mathrm{bi}}$. In this case, the current through the MOSFET is calculated using the following equation, which is originally derived for BJTs [12]:

$$I_{(t)} = q A \frac{D_{\mathrm{B}} n_{\mathrm{i}}^2}{W_{\mathrm{B}} N_{\mathrm{B}}} \left(e^{q \frac{V_{\mathrm{PB}} - \Phi_{\mathrm{bi}}}{K_{\mathrm{B}} T}} - 1\right). \tag{6}$$

If $V_{\mathrm{PB}} < \Phi_{\mathrm{bi}}$, the parasitic bipolar does not latch and the current through the MOSFET is determined by (1). Fig. 2 shows a schematic diagram illustrating how the electrothermal model works. Fig. 3(a) shows the trend of calculated normalized currents using the model in Fig. 2 at different ambient temperatures. Fig. 3 shows that the parasitic bipolar latches for higher ambient temperatures, but this is not the case for lower ones. The process of latching is characterized by a rising current, which in reality will be limited by the power supply, as will be demonstrated experimentally later on. Fig. 3(b) shows the calculated junction temperature of the MOSFET obtained from Fig. 2. It can be observed in Fig. 3(b) that there is a temperature rise resulting from the peak avalanche power. However, for the case of latchup, there is a subsequent temperature rise during the cooling period, which is due to

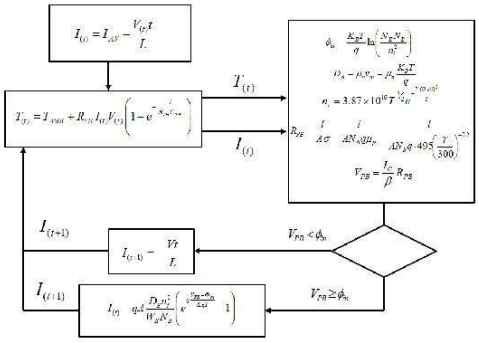

Fig. 2. Electrothermal model for parasitic BJT latchup for MOSFET in avalanche.

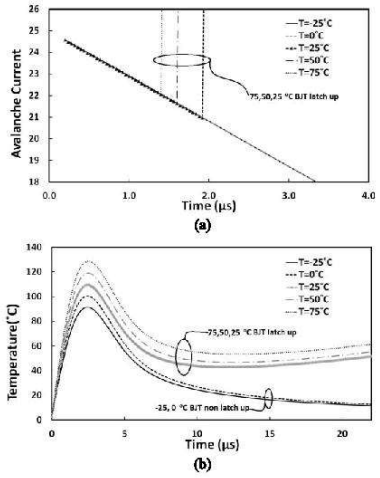

Fig. 3. (a) Calculated device current as a function of time at different ambient temperatures. (b) Calculated junction temperature as a function of time at different ambient temperatures.

the rising current from the activation of the parasitic BJT [1], [11]–[15]. With the detailed knowledge of device dimensions and process parameters, the calculations in Fig. 3(a) and (b) can be used by the designer as a predictor of BJT latchup for a specific device.

III. Experimental Measurements

A. Avalanche Performance at Fixed Currents

Fig. 4 shows the experimental setup and the circuit diagram that includes a gate-drive circuit, the environmental chamber, test enclosure, power supplies, and oscilloscopes. When the device under test (DUT) is switched ON, the inductor is charged to the peak avalanche current that is proportional to

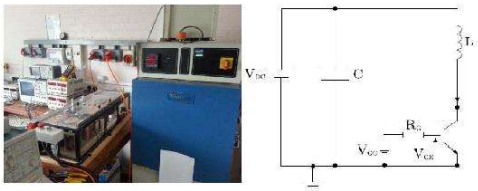

Fig. 4. Experimental setup showing UIS test and the circuit schematic diagram.

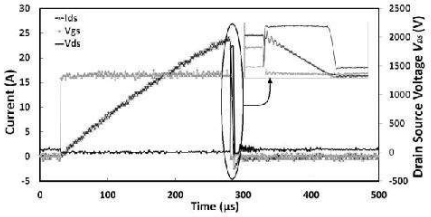

Fig. 5. V_{GS}, V_{DS}, and I_{DS} as functions of time for an SiC MOSFET under UIS.

the duration of the gate pulse. When the DUT is switched OFF, the current flowing through the inductor is interrupted, thereby causing the inductor to force current through the DUT. Since the DUT is OFF, current flows from the drain to the source through avalanche mode conduction. The drain–source voltage rises to a value that reaches the breakdown voltage as the current flows through the device [5], [16]. Fig. 5 shows the experimental measurements of the gate–source voltage (V_{GS}), the drain–source current (I_{DS}), and the drain–source voltage (V_{DS}) as functions of time for an SiC MOSFET undergoing UIS.

The devices used in the experiments were the 1.2-kV/24-A CREE SiC MOSFET with datasheet reference CMF10120D and the 1.2-kV/30-A Fairchild silicon IGBT with datasheet reference FGA15N120ANTD. The test was conducted at six different temperatures, namely −25 °C, 0 °C, 25 °C, 50 °C, 75 °C, and 100 °C. The performance of the device was examined under two different avalanche currents (24 and 35 A). The 35-A test exceeds the maximum forward current rating of the SiC MOSFET by 40% and the maximum current rating of the IGBT by 16%, thereby putting the SiC MOSFET under more electrothermal stress. Fig. 6(a) shows the drain–source voltage of the SiC MOSFET under UIS at the rated current for different temperatures.

Fig. 6(b) also shows the avalanche current characteristics of the SiC MOSFET at different temperatures. Fig. 6(c) shows the collector–emitter voltage of the IGBT under UIS, whereas Fig. 6(d) shows the collector–emitter current of the IGBT under UIS. The SiC MOSFET demonstrates temperature invariant characteristics and withstands all temperatures, whereas the silicon IGBT does not withstand the avalanche current at 100 °C, as can be observed in Fig. 6(c) and (d).

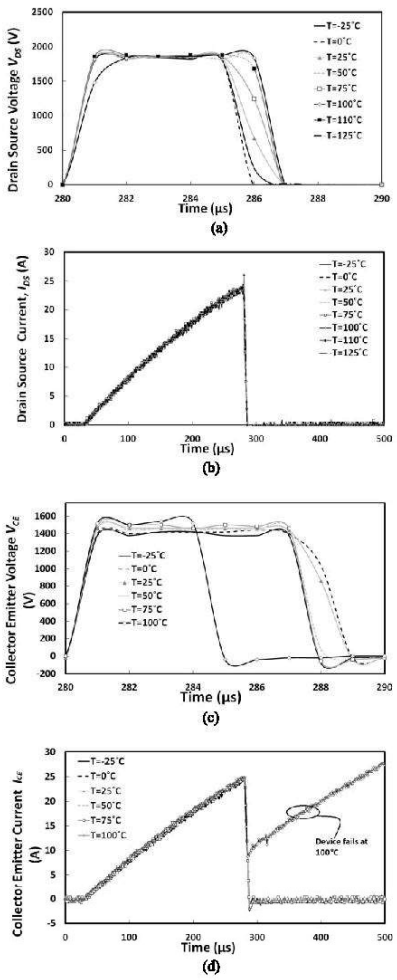

Fig. 6. (a) Drain–source voltage for the SiC MOSFET under UIS at different temperatures. (b) Drain–source current for the SiC MOSFET under UIS at different temperatures. (c) Collector–emitter voltage for the Si IGBT under UIS at different temperatures. (d) Collector–emitter current for the Si IGBT under UIS at different temperatures. Test current $I_L = 24$ A.

In Fig. 6(c), the V_{CE} of the IGBT collapses to zero at the moment the short circuit across the device occurs. In Fig. 6(d), the current through the IGBT at 100 °C rises uncontrollably, thereby indicating BJT latchup. Subsequent tests on the device show that all the terminals were short circuited and the device was damaged.

Next, the SiC MOSFET was tested at 40% beyond its current rating, whereas the IGBT was tested at 16% beyond its current rating to ascertain the electrothermal ruggedness.

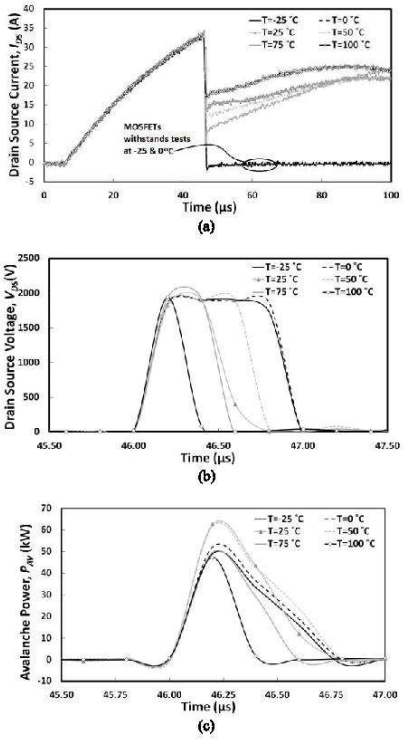

Fig. 7. (a) Drain–source current for the SiC MOSFET under UIS at different temperatures showing BJT latchup above 0 °C. (b) Drain–source voltage for the SiC MOSFET under UIS at different temperatures showing BJT latchup above 0 °C. (c) Avalanche power dissipated in the SiC MOSFET. Test current $I_L = 35$ A.

Fig. 7(a) shows the avalanche current characteristics of the SiC MOSFET under different temperatures. The MOSFET withstands the test at the low temperature measurements (−25 °C and 0 °C). For temperatures above 25 °C, the current rises and is limited by the power supply, i.e., the MOSFET goes into thermal runaway. Subsequent tests on the devices showed that they are shorted between all three terminals, indicating that the devices had failed. The mechanism behind the temperature dependency of the devices ability to withstand UIS can be explained by Figs. 2 and 3. Fig. 7(b) shows the corresponding drain–source voltage (V_{DS}), where it can be seen that V_{DS} falls to zero more quickly as the temperature is increased. This occurs as a result of the fact that the voltage across the device collapses once the bipolar has latched.

Fig. 7(c) shows the avalanche power dissipated by the SiC MOSFET at different ambient temperatures. The amount of power dissipated by the device before the onset of the BJT latchup increases as the temperature decreases. This can be explained by the fact that dissipated power contributes to

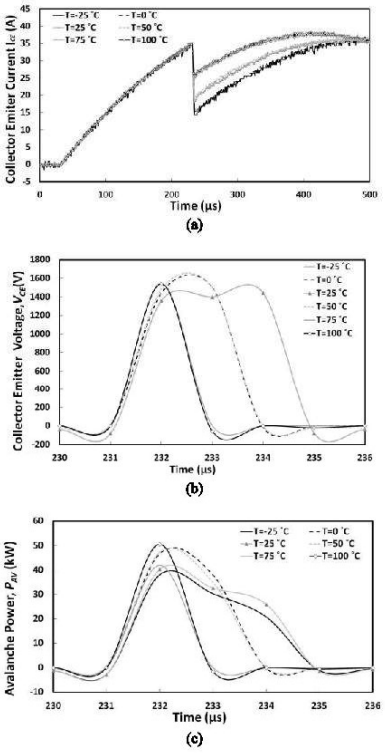

Fig. 8. (a) Collector–emitter current for the silicon IGBT under UIS at different temperatures. (b) Collector–emitter voltage for the silicon IGBT under UIS at different temperatures. (c) Avalanche power dissipated in the silicon IGBT. Test current $I_L = 35$ A.

temperature excursions within the device, and hence, when the device starts at a lower ambient temperature, there is more headroom to dissipate power before bipolar latchup. Fig. 7 is thus the experimental validation of Fig. 3 and the model developed for BJT latchup in Section II.

Fig. 8(a) shows the collector–emitter current of the silicon IGBT under UIS conditions with 35-A maximum avalanche current. It can be seen that unlike the SiC MOSFET, the silicon IGBT does not withstand the test at any temperature. A trend can also be noticed from the IGBT current. The latchup current (i.e., the current flowing through the device at the point when latchup occurs) increases with increasing temperature. Fig. 8(b) shows the collector–emitter voltage of the IGBT under UIS conditions at all the temperatures. Similar to the MOSFETs, the voltage across the device collapses to zero once the device latches. Fig. 8(c) shows the avalanche power dissipated before the onset of thermal runaway. The amount of avalanche power dissipated before the parasitic BJT latchup decreases with increasing temperature.

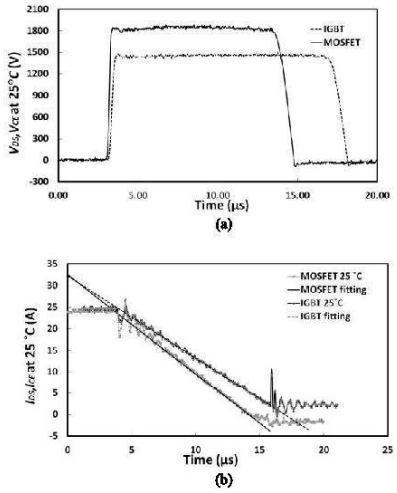

Fig. 9. (a) V_{DS} and V_{CE} for the IGBT and the MOSFET during avalanche mode conduction. (b) I_{DS} and I_{CE} for the IGBT and the MOSFET during avalanche mode conduction. Test current $I_L = 35$ A.

Fig. 9(a) shows the V_{CE} and V_{DS} characteristics of the IGBT and the MOSFET, respectively, during avalanche. It can be seen that the MOSFET has a higher breakdown voltage than the IGBT even though both devices are rated at 1.2 kV. Fig. 9(b) shows that the gradient of the avalanche current is higher for the IGBT. This happens because of the higher breakdown voltage of the MOSFET since $t = \mathrm{LI_{AV}}/(B_{\mathrm{VDSS}} - V_{\mathrm{DS}})$, where B_{VDSS} is the breakdown voltage, I_{AV} is the avalanche current, and t is the time. Hence, Fig. 9(b) shows that the avalanche current decreases as the avalanche duration increases.

B. Maximum Avalanche Current Determination

In this section of the experimental measurements, the goal is to determine the maximum avalanche current at a fixed temperature and fixed inductor (avalanche duration). This is done by increasing the pulse duration of the gate until device failure is initiated since the width of the gate pulse determines the peak avalanche current. The results of the measurements therefore show the peak avalanche current sustainable by the device. This test is conducted for both the SiC MOSFET and the silicon IGBT at different temperatures. Fig. 10 shows the experimental measurements of different peak avalanche currents for the SiC MOSFET at room temperature. The measurements show that extending the gate pulse gradually will eventually cause device failure when the peak avalanche current is reached at that specific temperature.

Fig. 11(a) shows the peak avalance current when the Si IGBT fails at different temperatures. Fig. 11(b) shows the equivalent results for the SiC MOSFET. It can be seen from both plots that the maximum avalanche current reduces with

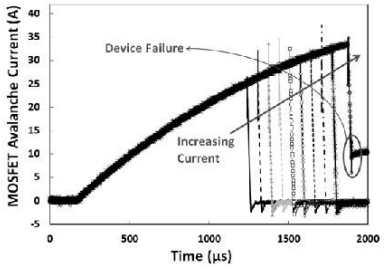

Fig. 10. Avalanche current as a function of time for different gate pulses showing the maximum avalanche current for SiC MOSFET.

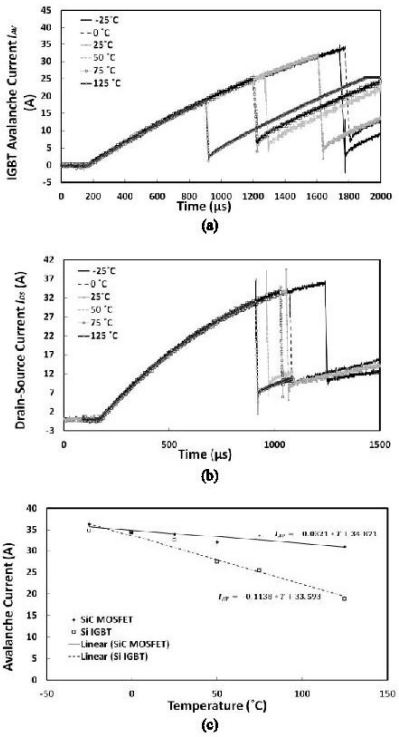

Fig. 11. (a) IGBT peak avalanche current as a function of time for different temperatures. (b) MOSFET peak avalanche current as a function of time for different temperatures. (c) Peak avalanche current as a function of temperature for the MOSFET and the IGBT.

increasing temperature for reasons explained earlier. The total charging time of the MOSFET is smaller than that of the IGBT as a result of the smaller ON-state resistance. Hence, less time is required for the device to reach a defined avalanche current. Fig. 11(c) shows the peak avalanche current sustained by the device before latchup as a function of temperature for both the silicon IGBT and the SiC MOSFET.

It can be observed that the absolute value of the slope of the maximum I_{AV} versus temperature is higher for the silicon IGBT, thereby indicating a less reliable device at elevated temperatures, i.e., there is greater temperature dependency of electothermal ruggedness in the IGBT than the MOSFET. The slope in Fig. 11(c) is -0.114 A/ °C for the silicon IGBT and -0.031 A/ °C for the SiC MOSFET. The x-axis intercept of Fig. 11(c) is an indication of the maximum operating temperature of the device. At this point, the elevated temperature causes enough thermal generation of carriers (through bandgap narrowing) that the carrier population is now equal to the background doping of the device, i.e., the device ceases to be a semiconductor. The extrapolated maximum operating temperature (x-axis intercept) for the silicon IGBT and the SiC MOSFET is 295 °C (568 K) and 1086 °C (1360 K), respectively. However, in reality, the device will fail long before the theoretical point as a result of process imperfections leading to current crowding and heat nonuniformity. This means that some parts of the MOSFET die will be at much higher temperatures compared with others. Furthermore, packaging constraints will further limit the maximum junction temperature to a value significantly lower than what the semiconductor device is capable of. It can be observed from Fig. 11(c) that the SiC device has a much higher maximum operating temperature by virtue of wider bandgap. The intrinsic carrier concentration can be calculated for silicon and SiC from the following [12]:

$$n_{\mathrm{i}} = 3.87 \times 10^{16}\ T^{3/2} \exp\left(-\frac{7.02 \times 10^{3}}{T}\right) \tag{7}$$

$$n_{\mathrm{i}} = 1.7 \times 10^{16}\ T^{3/2} \exp\left(-\frac{2.08 \times 10^{4}}{T}\right). \tag{8}$$

At 295 °C, the calculated intrinsic carrier concentration for silicon is 2.25×10^{15} cm^{-3}, whereas at 1086 °C, the calculated intrinsic carrier concentration for SiC is 1.92×10^{14} cm^{-3}. Hence, it is clear that the widebandgap of SiC enables better electrothermal ruggedness since the thermally generated carrier concentration for SiC is less than that of silicon even when the ambient temperature is 3.5 times higher [17].

IV. Finite-Element Models

Finite-element models have been developed to describe SiC MOSFET and silicon IGBT behavior under avalanche mode conditions. ATLAS from SILVACO was used to investigate the electrothermal behavior of the MOSFET during avalanche. The SiC device in the simulation was optimized to yield a breakdown voltage of 1200 V using an 8-μm depletion layer with a doping of 2×10^{16} cm^{-3}. The p-body doping and n-source was 1×10^{17} and 2×10^{19} cm^{-3}, respectively. The silicon IGBT is simulated with a drift layer doping of 1.1×10^{14} cm^{-3}, a p-body doping of 2.3×10^{17} cm^{-3}, and a voltage blocking drift layer thickness of 100 μm. The circuit in the simulator was identical to the one used in the experiment. The results of the simulations are shown in Fig. 12(a)–(c) for both the MOSFET and the IGBT.

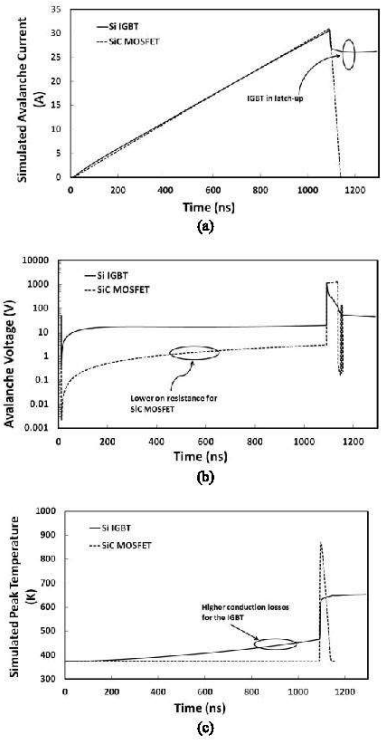

Fig. 12. (a) Simulated avalanche current as a function of time for the SiC MOSFET and the silicon IGBT. (b) Simulated avalanche voltage as a function of time for the SiC MOSFET and the silicon IGBT. (c) Simulated maximum temperature as a function of time for the SiC MOSFET and the silicon IGBT.

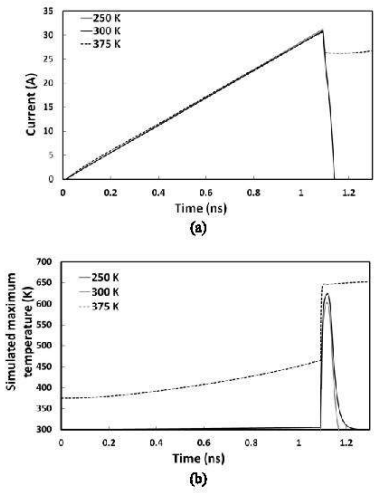

Fig. 13. (a) Simulated IGBT current during inductor charging and avalanche at different ambient temperatures. (b) Simulated IGBT voltage during inductor charging and avalanche at different ambient temperatures.

Fig. 12(a) shows the avalanche current as a function of time for the MOSFET and the IGBT. The ambient temperature of the simulation is 473 K, and the avalanche current is 35 A. It can be observed from Fig. 12(a) that the IGBT goes into latchup, whereas the MOSFET does not. Fig. 12(b) shows the voltage across the device as a function of time for both the SiC MOSFET and the silicon IGBT. It can be observed that the IGBT has a higher voltage during the inductor charging period than the MOSFET. This is due to the higher ON-state resistance of the IGBT as a result of the thicker drift layer compared with the SiC MOSFET, where the widebandgap and high critical field mean that a thinner voltage blocking epitaxial layer is needed. The modeled characteristics of the voltage of the device during avalanche is identical to what is observed experimentally, i.e., once the device goes into avalanche mode conduction, the voltage across the device rises to the breakdown voltage, and if the device latches, the voltage across the device falls to zero as the current rises. Fig. 12(c) shows the simulated maximum temperature of the device as a function of time during the inductor charging and the avalanche period.

The IGBT shows a higher temperature rise during the inductor charging period as a result of the higher conduction losses compared with the SiC MOSFET. The rise of the SiC MOSFET temperature during avalanche is faster and the peak temperature is higher because of the smaller thermal time constant. The simulated SiC MOSFET will have a smaller thermal resistance (R_{TH}) because of the thinner epitaxial drift layer (thermal resistance increases with length in the direction of heat flow). SiC also has a thermal conductivity that is three times larger than silicon, and hence, the thermal resistance would reduce even further. The SiC MOSFET will also have a smaller heat capacitance (C_{TH}) as a result of the smaller die mass. Therefore, the smaller thermal time constant ($R_{\mathrm{TH}} \cdot C_{\mathrm{TH}}$) means that the rate of change of temperature with time will be higher, and hence, the faster heating and cooling shown in Fig. 12(c). It can also be seen in Fig. 12(c) that the IGBT never cools down unlike the SiC MOSFET. Fig. 13 shows more finite-element simulations for the silicon IGBT during inductor charging and avalanche mode conduction at different ambient temperatures. It can be observed from Fig. 13 that, similar to the case of the experimental measurements, higher temperatures induce latchup. Furthermore, in the finite-element analysis, the latchup occurs approximately at 650 K that is higher than what was extracted experimentally (568 K) by extrapolating the plots in Fig. 11(c). This is expected since the simulation does not take into consideration process imperfections and packaging constraints.

2-D current density contour plots of the SiC MOSFET and silicon IGBT were also extracted from the finite-element

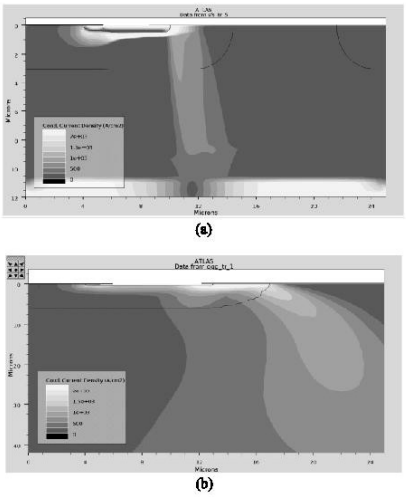

Fig. 14. 2-D current density plots for the (a) SiC MOSFET and (b) silicon IGBT.

simulator. The results are shown in Fig. 14(a) for the MOSFET and Fig. 14(b) for the IGBT. In the case of the MOSFET, the current flow is concentrated, whereas in the IGBT, the current flow is dispersed. This is likely due to the fact that the voltage blocking drift layer of the SiC MOSFET is much thinner than that of the IGBT as a result of the higher critical electric field in SiC. The lower value of the thermal time constant of SiC means that heat is dissipated faster than that of silicon; hence, the temperature surge does not initiate bipolar latchup as is the case with the IGBT.

V. Conclusion

In this paper, the mechanism of parasitic bipolar latchup during avalanche mode conduction has been investigated for 1.2-kV/25-A SiC MOSFETs and 1.2-kV/30-A silicon IGBTs. It has been shown that the SiC MOSFET is more electrothermally rugged and can withstand higher temperature surges in spite of the fact that it has a lower current rating. The SiC device can withstand avalanche current 40% greater than the rated current at lower temperatures but not at higher temperatures. The IGBT is unable to withstand avalanche currents 16% beyond its rating. The SiC MOSFET can also withstand avalanche currents at the rated value at 125 °C. An electrothermal model was developed that explained why elevated temperatures accelerate the latching of the parasitic BJT, and the results are confirmed by finite-element modeling. The experimentally extracted maximum operation temperatures (extracted from avalanche current versus temperature plots) were compared with theoretical calculations using the temperature dependence of the intrinsic carrier concentration. The results showed a difference probably due to packaging constraints and process imperfections and that the SiC device is capable of withstanding approximately three times the temperature of Si. This was also supported by the finite-element models.

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Analysis of Power Device Failure Under Avalanche Mode Conduction

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***Abstract*– This paper investigates the physics of device failure during avalanche for 1.2 kV SiC MOSFETs, silicon MOSFETs and silicon IGBTs. The impact of ambient temperature, initial conditions of the device prior to avalanche breakdown and the avalanche duration is explored for the different technologies. Two types of tests were conducted namely (i) constant avalanche duration with different peak avalanche currents and (ii) constant peak avalanche current with different avalanche durations. SiC MOSFETs are shown to be the most rugged technology followed by the silicon IGBT and the silicon MOSFET. The material properties of SiC suppress the triggering of the parasitic BJT that causes thermal runaway during avalanche.**

***Index Terms*—Avalanche Conduction, MOSFET, Reliability, Silicon Carbide,**

I. Introduction

It is important for power devices to be able to conduct current in avalanche reliably without suffering thermal destruction. Some applications such as the Integrated-Starter-Alternator in automotive systems use low on-state resistance MOSFETs in avalanche mode, hence, device reliability under these conditions is critical [1, 2]. There are two avalanche conduction modes, namely static and dynamic. In the static avalanche case, the device is in the normal forward conduction mode, hence, the voltage across the device is low while the current is high. In the case of dynamic latching, both the voltage and current are high which can happen during linear mode operation and unclamped inductive switching. The current density for dynamic avalanche to occur is less than that of the static [3-5]. The ambient temperature is critical in determining the avalanche capability of the device and largely causes the device to operate less reliably as it is increased [6]. Depending on the peak avalanche current and the avalanche duration (size of the inductor storing energy), the power device will dissipate different amounts of avalanche energy reliably [7]. The avalanche capabilities of power devices will also depend on the transistor technology type as well as the fabrication material. In this paper the avalanche capabilities of 1.2 kV SiC MOSFETs, Si IGBTs and Si MOSFETs is examined. Two different circuits were used for conducting the experiments as well as several avalanche energies and ambient temperatures. In section II the experimental set up is described and the measurements are presented. In Section III, the junction temperatures are calculated and the conclusions are presented in section IV.

II. EXPERIMENTAL SETUP UP AND MEASUREMENTS

The experiments were conducted using the equipment shown in Fig.1.

Fig. 1. Experimental set up

The experiments were undertaken using CREEs SiC MOSFET (CMF10120D), Fairchild's silicon IGBT (FGA15N120ANTD) and IXYS silicon MOSFET (IXFX20N120). All of the devices are rated at 1.2 kV and similar current ratings. The avalanche durations were modulated using 4 different inductor sizes namely 1.2 mH, 2.2 mH, 4.8 mH and 9.5 mH. The devices were placed in an environmental chamber in order to modulate different ambient temperatures and observe the impact of temperature. The tests were conducted at -25˚C, 0 ˚C, 25˚C, 50 ˚C, 75 ˚C and 125 ˚C.

Two different circuit configurations were used in the avalanche experiments. In one configuration shown in Fig. 2(a), the DUT is used to charge the inductor which means there is some initial current through the device when it is set into avalanche. In the second configuration shown in Fig. 2(b), a different higher voltage device is used to charge the inductor meaning the DUT is never switched on. In the tests conducted using the circuit in Fig. 2(a), there will be some initial junction temperature rise in the DUT due to the fact that there is some initial current in the channel of the device, hence, some conduction losses. In the experiments in Fig. 2(b), the initial junction temperature will be the ambient temperature

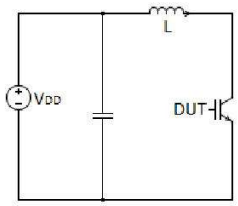

Fig. 2(a). Circuit with DUT charging the inductor

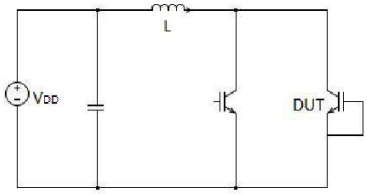

Fig. 2(b). Circuit with DUT not charging the inductor

Fig. 3 shows a typical measurement of the avalanche characteristics using the circuit in Fig. 2(a), where it can be seen that there is simultaneously high voltage across and current through the device while the inductor dissipates current into the DUT. This voltage is the breakdown voltage of the device.

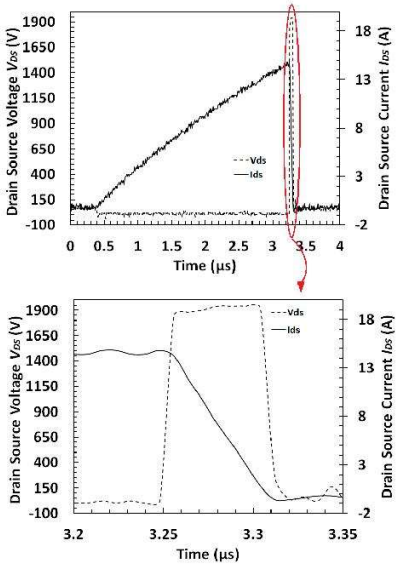

Fig. 3. Device Charging Inductor and going into avalanche

A. DUT charging the inductor (Test circuit in Fig. 2(a) i.e. DUT gate is ungrounded)

The first test was conducted using the circuit of Fig. 2 (a). The results presented in the following figures are for both the MOSFETS and the IGBTs for all the inductances and all the temperatures used. To calculate avalanche energy, the following formula was used:

$$E_{AV} = \frac{1}{2} L I_{AV}^{\ 2}$$

where E_{AV} is the avalanche energy, L is the inductance and I_{AV} is the peak avalanche current. Fig. 4 shows the calculated peak avalanche energy (prior to device failure) as a function of temperature for different avalanche durations (inductances) for the SiC MOSFET. Similar results for the IGBT are presented in Fig. 5. It can be seen that the peak avalanche energy decreases with temperature as expected because the initial junction temperature sets the headroom for the amount of energy to be dissipated.

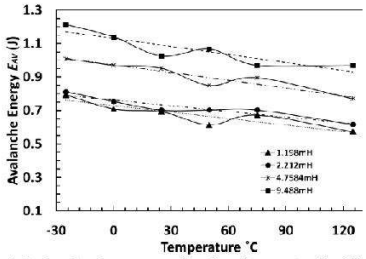

Fig. 4. Peak avalanche energy as a function of temperature for different inductances for the SiC MOSFET

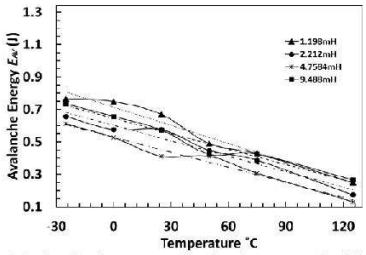

Fig. 5. Peak avalanche energy as a function of temperature for different inductances for the Silicon IGBT

From Fig. 4 and Fig. 5, it can be seen that the SiC MOSFET is capable of withstanding higher peak avalanche energy compared to the silicon IGBT and that the difference between them increases with the avalanche duration. In the case of the SiC MOSFET, the maximum avalanche energy conducted by the device increases with the avalanche duration whereas for the IGBT, the

maximum avalanche energy is somewhat less dependent on the inductances used.

There are 2 failure modes explored in the experiments. The first failure mode is low avalanche duration with higher avalanche currents while the second failure mode is low avalanche currents with higher avalanche durations. Although both tests are designed to evaluate the electrothermal ruggedness of the devices, the first test evaluates the resistance of the device to latch-up (BJT latch-up for the MOSFET and Thyristor latch-up for the IGBT) while the second test evaluates the maximum intrinsic temperature that the device is capable of sustaining. Parasitic BJT latch-up is also influenced by an unequal temperature distribution across the chip resulting from parametric variability between the cells in the power device. In the 1st failure mode, since the avalanche duration is short and there is insufficient time for the chip temperature to rise uniformly, hot-spotting will contribute significantly to device failure via BJT latch-up. In other words, the electrical time constant of the chip is much smaller than the thermal time constant so the failure mode is primarily an electrical switching mode. Hence, devices with manufacturing defects will fail this test rapidly before the chip has a chance to reach its thermal limits. In the 2nd failure mode, the avalanche duration is long enough and the initial power is small enough to allow uniform temperature rise across the chip. Hence, the thermal time constant of the chip is comparable to the electrical time constant of the switching event and the temperature limits of the device are tested. It is known that the intrinsic temperature limit of the device is reached when the thermally generated carriers due to temperature induced bandgap narrowing becomes equal to the background doping of the device. Fig. 6 to Fig. 9 shows the maximum avalanche energy dissipated prior to device failure for both the SiC MOSFET and the silicon IGBTs with different avalanche durations (inductances). The inductance used in Fig. 6 is the 1.2 mH, in Fig. 7 is 2.2 mH, in Fig. 8 is 4.8 mH and in Fig. 9 is 9.5 mH.

It can be seen that for the measurements made with the smaller inductances (Fig. 6 and Fig. 7), the difference in electro-thermal ruggedness (maximum avalanche energy prior to device failure) between the two technologies is smaller compared to the measurements made using the larger inductances. As the avalanche duration (inductor) is increased, the failure mode changes from latch-up to intrinsic temperature limitations, hence, the performance of the SiC MOSFET relative to the silicon IGBT improves. It can be seen from the measurements made using the larger inductances (Fig. 8 and Fig. 9) that the SiC MOSFET is significantly more avalanche rugged as the avalanche duration is increased. This is due to the higher intrinsic temperature capability of the device owing to its larger bandgap i.e. due to the larger bandgap, the rate of carrier generation with temperature is less for the SiC device hence, the device is more resistant to thermal runaway.

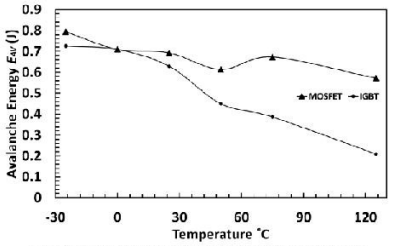

Fig. 6. Energy Comparison between MOSFET IGBT using L=1.2 mH

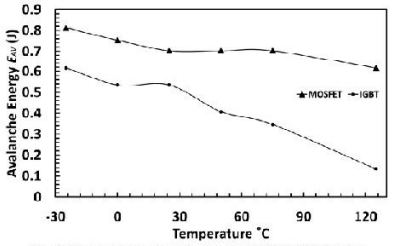

Fig. 7. Energy Comparison between MOSFET IGBT using L=2.2 mH

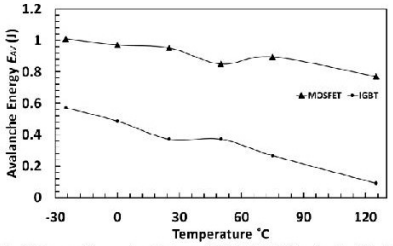

Fig. 8. Energy Comparison between MOSFET IGBT using L=4.8 mH

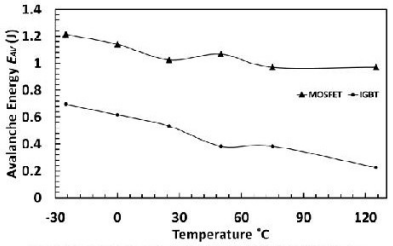

Fig. 9. Energy Comparison between MOSFET IGBT using L=9.5 mH

B. DUT not charging the inductor (Test circuit in Fig. 2(b)i.e. DUT gate is grounded)

In the second part of the experiment, the avalanche inductor was charged using a high breakdown voltage device while the gate of the DUT was grounded to the source. In other words, the DUT is never switched on. The circuit diagram used is shown in Fig. 2b. The high voltage device used was IXEL 40N400-N with a breakdown voltage of 4 kV and current capability of 90 A. Since the avalanche current will always flow through the device with the lower breakdown voltage rating, the high voltage device would not interfere with the avalanche measurements. The breakdown voltage of the device was not affected by grounding the gate. Also, the breakdown voltage difference between the silicon IGBT and the SiC MOSFET remained the same [8]. The results for the avalanche current and the avalanche energy for the MOSFET are shown in Fig. 10 and for the IGBT in Fig. 11. Fig. 10(a) shows the maximum avalanche current as a function of temperature for the SiC MOSFET using the 1.2 mH inductance. Fig. 10(a) compares the electrothermal ruggedness for the case of the DUT used to charge the inductor (circuit in Fig. 2a where the gate is ungrounded) and the case where the gate of the DUT is grounded (circuit in Fig. 2b where the DUT is grounded and never switched on). Fig. 10(b) shows a similar plot for the SiC MOSFET with the avalanche energy shown as a function of the ambient temperature. It can be seen, as expected, that the electrothermal ruggedness is higher using the circuit configuration in Fig. 2(b) where the gate of the DUT is grounded. In fact, when the gate of the DUT is grounded, the SiC MOSFET never fails so the points shown in Fig. 10(a) and Fig. 10(b) represent the limits of the test equipment as shown in the figure.

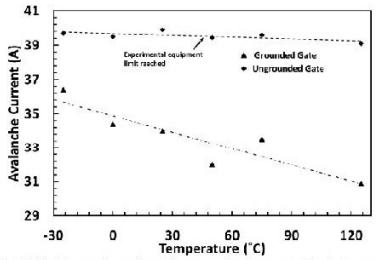

Fig. 10(a). Comparison of maximum avalanche current I_{AV} between grounded and non-grounded gate for the SiC MOSFET

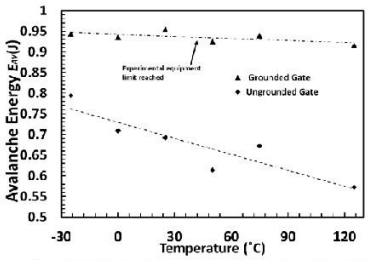

Fig. 10(b). Comparison of maximum avalanche energy E_{AV} between grounded and non-grounded gate for the SiC MOSFET

For the SiC MOSFET, it is clear that there is a major difference between the two configurations. With the gate of the SiC MOSFET grounded, there was insufficient energy to trigger BJT latch-up and thermal runaway in the device hence, the maximum avalanche energy the SiC MOSFET is capable of reliably dissipating is unknown for that particular test configuration. The limits of the test equipment were reached.

Similar results are shown for the silicon IGBT in Fig.11(a) where the peak avalanche current is shown as a function of temperature and in Fig. 11(b) where the peak avalanche energy is shown as a function of temperature. As was done for the SiC MOSFET in Fig. 10, comparisons have been made for the silicon IGBT between measurements with the ungrounded gate (using the circuit in Fig. 2a where the DUT charges the inductor) and grounded gate where DUT is never switched (Fig. 2b where another device charges the inductor). As expected, higher temperatures reduce the avalanche ruggedness performance of the DUTs. However, unlike the case of the SiC MOSFETs, there is not a substantial difference between the 2 tests (grounded gate vs ungrounded gate). In other words, using the DUT to charge the inductor does not yield avalanche ruggedness capability results that are significantly less than using a higher voltage transistor to charge the inductor.

Hence, Fig. 10 and Fig. 11 show that grounding the gate for the SiC MOSFET completely suppressed the mechanism of BJT latch-up and the devices were indestructible using the experimental set-up. However, for the silicon IGBT, grounding the gate had no impact on the mechanism of thyristor latch-up. It is thought that the material properties of SiC were key to this observation since similar measurements on 1.2 kV silicon MOSFETs showed significantly less electrothermal ruggedness for all test conditions.

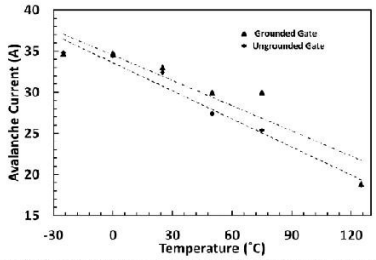

Fig. 11(a). Comparison of the maximum avalanche current I_{AV} between grounded and non-grounded gate for the silicon IGBT

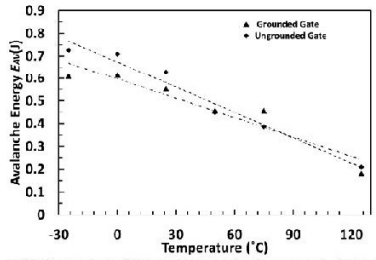

Fig. 11(b). Comparison of the maximum avalanche energy E_{AV} between grounded and non-grounded gate for the silicon IGBT

To ensure that the breakdown voltage characteristics of the DUT have been unaffected by the addition of the charging transistor, the drain-source characteristics of the DUT were monitored during avalanche for the case of the grounded and non-grounded gate measurements. The drain-source voltage characteristics during avalanche are shown in Fig. 12(a) for SiC MOSFET under both test conditions where it can be seen that the breakdown voltage does not change. Fig. 12(b) shows a similar plot for the silicon IGBT. Fig. 12(c) shows the drain-source voltage characteristics for the silicon IGBT and SiC MOSFET during avalanche where it can be seen that the breakdown voltage is higher for the SiC MOSFET and the avalanche duration is shorter. It should be noted that all the measurements are with the same inductor. The longer avalanche duration in the SiC MOSFET is due to the higher breakdown voltage.

Similar avalanche ruggedness tests have been carried out on the 1.2 kV silicon MOSFETs. Fig. 13 shows the maximum avalanche current as a function of temperature for the 3 technologies namely, the SiC MOSFET, the silicon IGBT and the silicon MOSFET all rated a 1.2 kV. In Fig. 13, all of the measurements have been carried out on the 9.5 mH inductor with the DUT not used to charge the inductor i.e. the gate of the DUT is grounded and a high voltage transistor is used to charge the inductor. From Fig.13 it is evident that the most resilient device is the SiC MOSFET followed by the silicon IGBT and the Si MOSFET. The dependency of the avalanche ruggedness capability on temperature is more or less similar between the two MOSFETs probably due to the same architecture. The silicon IGBT exhibits a higher temperature dependency with the maximum avalanche current decreasing much more rapidly as the temperature is increased. The differentiating factor between the MOSFETs capability is the superior electrothermal capability of silicon carbide.

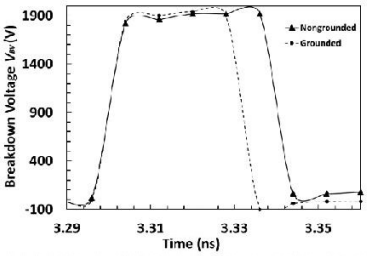

Fig. 12(a). Drain-source voltage characteristics of the SiC MOSFET during avalanche with both circuit configurations

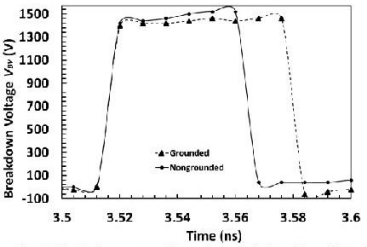

Fig. 12(b). Drain-source voltage characteristics of the silicon IGBT during avalanche with both circuit configurations

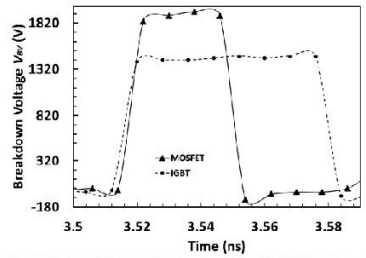

Fig. 12(c). Breakdown voltage of IGBT and MOSFET with grounded gates on both devices

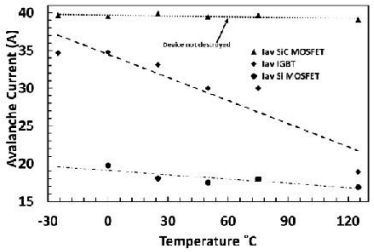

Fig. 13. Avalanche current for SiC MOSFET, Si IGBT, Si MOSFET with grounded gates

III. Junction Temperature Calculation

Due to the nature of the test, it is very difficult to measure the junction temperature of the device using temperature sensitive electrical parameters during avalanche. However, the temperature can be calculated using electro-thermal equations that have been calibrated by finite element models. Using [9] it is possible to calculate the junction temperature when the device is in avalanche. The temperature is calculated using

$$T_J@n * \frac{t_{AV}}{10} = \begin{cases} \frac{P_O * K}{10} * \sqrt{\frac{t_{AV}}{10}} * \left[10 * \sqrt{n} - \sum_{1}^{n} \sqrt{n}\right], n \leq 10 \\ \frac{P_O * K}{10} * \sqrt{\frac{t_{AV}}{10}} * \left[10 * \sqrt{n} - \sum_{n-9}^{n} \sqrt{n}\right], n > 10 \end{cases}$$

Where T_J is the junction temperature, t_{AV} is the duration of the avalanche which is extrapolated from the measurements, P_O is the peak power also calculated from the measurements, K refers to the device thermal response and is calculated from the transient thermal impedance characteristic provided in the data sheet, n is the time step of the calculated temperature. The transient thermal characteristics for different ambient temperatures during avalanche for the SiC MOSFET are presented in Fig.14. The inductor used for the measurements in Fig. 14 was 9.5 mH. Fig. 15 shows the temperature transient characteristics for the SiC MOSFET during avalanche with different inductors (i.e. different avalanche durations). The ambient temperature used in the calculations of Fig. 15 was 25°C. Fig. 16 and Fig. 17 show similar calculated thermal transients for the silicon IGBT.

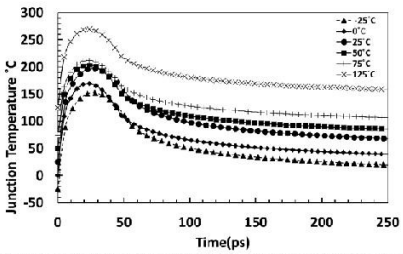

Fig. 14. Junction Temperature for SiC MOSFET for different ambient temperatures

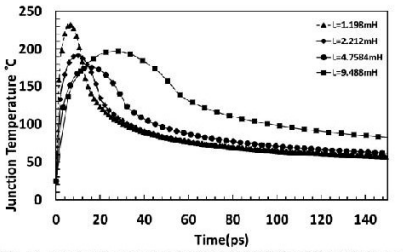

Fig. 15. Junction Temperature for SiC MOSFET for different inductors

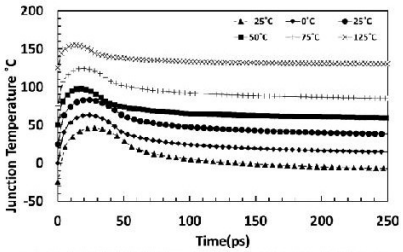

Fig. 16. Junction Temperature for Si IGBT for different ambient temperatures

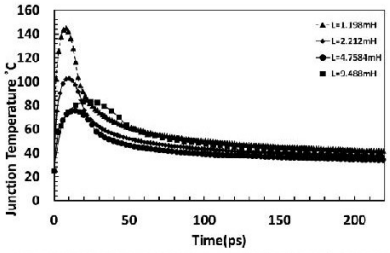

Fig. 17. Junction Temperature for Si IGBT for different inductors

Fig. 18 shows the peak calculated junction temperature for the SiC MOSFET and silicon IGBT at different ambient temperatures where a linear relationship can be

observed. Fig. 19 shows the peak junction temperature for both technologies with different inductors at 25 C.

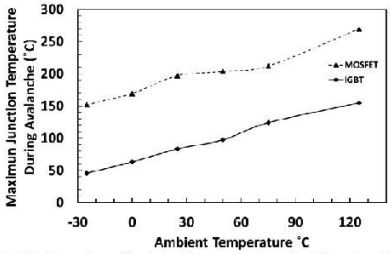

Fig. 18. Comparison of peak junction temperatures for different ambient temperatures

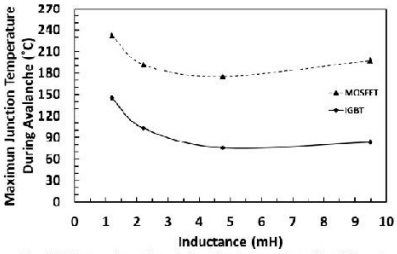

Fig. 19. Comparison of peek junction temperatures for different inductances

Regardless that the junction temperature of the SiC MOSFET is higher than that of the Si IGBT the MOSFET is more resilient to avalanche. The thermal capabilities of SiC are the dominant factor for the avalanche capabilities of the device

IV. Conclusions

Power device failure under unclamped inductive switching can be triggered under two conditions namely, high avalanche current with a short avalanche duration (condition A) and a low avalanche current with a long avalanche duration (condition B). Under condition A, parasitic BJT latch-up due to hot-spotting resulting from an unequal temperature distribution and inter-cell parametric variation within the power device, is known to be the trigger mechanism. Whereas under condition B, the intrinsic semiconductor temperature limitation resulting from thermally induced bandgap narrowing is thought to be the trigger mechanism. In this paper, SiC power MOSFETs are shown to be more avalanche rugged under condition B for the same avalanche energy compared to condition A. In the case of IGBTs, there is not a significant difference between the two conditions as far as the maximum avalanche energy is concerned. UIS tests have also been performed when the DUT is used to pre-charge the inductor (condition C) and when another device is used to pre-charge the inductor while the gate of the DUT is clamped to its source (condition D). SiC power MOSFETs are shown to be significantly more rugged in condition D compared to condition C. The results show that the material property of the semiconductor is more critical for determining avalanche mode ruggedness than the device type.

V. Acknowledgment

This work was supported by the EPSRC national centre of power electronics on the devices theme project (EP/L007010/1) and the components theme project (EP/K034804/1).

VI. References

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8.1.Dependence of Vds from Ls

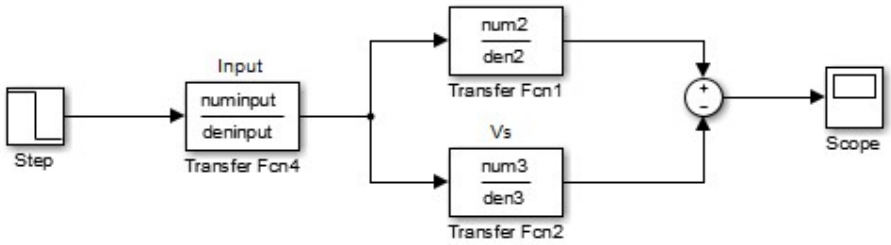
```
clc
clear all
close all
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Setting the symbols
syms Vd Vg Vs s Cgd Cgs Ld Lg Ls Vdd Vgg Cgd Cgs Rg Rdson
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Lsi=[0.1 0.2 0.3 0.4 0.5 ];
l=length(Lsi);
for i=[1:l]

    Ls=Lsi(i)*1e-6;

%Setting the values
% Ld=1e-9;  Lg=1e-8; Cgs=0.1e-9; Cgd=10e-9;  Rg=22; Vgg=0; Vdd=200;
%  Rdson=200;
% % % % % %  Ld=1e-10; Lg=1e-10; Cgs=0.7e-10; Cgd=1e-11; Vgg=1; Vdd=200;
% % % % % % gfs=1e-3; Vth=5; Ls=30e-6;Rg=22;
Ld=10e-9; Lg=10e-9; Cgs=4e-9; Cgd=2.5e-9; Vgg=0; Vdd=190;
gfs=1e-3; Vth=5; Rg=22; Rdson=400;
%  Ld=1e-12;  Ls=1000e-12;  Lg=1e-12;  Cgs=0.6e-12;  Cgd=1e-13;  Rg=20e-3;  Vgg=20;
Vdd=200;
% gfs=1e-3; Vth=5; Rdson=10e-3;
%%
numinput=[0 1];
deninput=[Rg*Cgd 1];
input=tf(numinput,deninput);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% The transfer function for Vg %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%numerator
A=Cgd*Cgs*Lg*Ls*Rdson*Vdd + Cgd*Cgs*Ld*Ls*Rdson*Vgg;
B=Cgd*Lg*Ls*Vdd   +   Cgd*Ld*Ls*Vgg   +   Cgs*Lg*Ls*Vdd   +   Cgs*Ld*Ls*Vgg   +
Cgd*Cgs*Ls*Rdson*Rg*Vdd;
C=Cgd*Lg*Rdson*Vdd  +  Cgd*Ld*Rdson*Vgg  +  Cgd*Ls*Rg*Vdd  +  Cgs*Ls*Rg*Vdd  +
Cgs*Ls*Rdson*Vgg;
D=Ld*Vgg + Ls*Vgg + Cgd*Rdson*Rg*Vdd;
E=Rdson*Vgg;

%denumerator
A1=Cgd*Cgs*Ld*Lg*Rdson + Cgd*Cgs*Ld*Ls*Rdson + Cgd*Cgs*Lg*Ls*Rdson;
B1=Cgd*Ld*Lg  +  Cgs*Ld*Lg  +  Cgd*Ld*Ls  +  Cgs*Ld*Ls  +  Cgd*Lg*Ls  +  Cgs*Lg*Ls  +
Cgd*Cgs*Ld*Rdson*Rg + Cgd*Cgs*Ls*Rdson*Rg;
C1=Cgd*Ld*Rdson  +  Cgd*Ld*Rg  +  Cgs*Ld*Rg  +  Cgd*Lg*Rdson  +  Cgs*Lg*Rdson  +
Cgs*Ls*Rdson + Cgd*Ls*Rg + Cgs*Ls*Rg;
D1=Ld + Ls + Cgd*Rdson*Rg + Cgs*Rdson*Rg;
E1=Rdson;
num1=[A B C D E];, den1=[A1 B1 C1 D1 E1];
Vg=tf(num1,den1);
fprintf('Vg= '),Vg,fprintf('\n\n')
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% The transfer function for Vd %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%% W A R N I N G %%%%%%%%%%%%%
% Ld must have a non zero value for us to get a non zero transfer function
```

```
  %  Ld=1000e-9;  Ls=1000e-9;  Lg=1000e-9;  Cgs=0.2e-9;  Cgd=1e-12;  Rg=20;  Vgg=20;
Vdd=0;
  % gfs=1e-3; Vth=5; Rdson=1000;
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %numerator
  A=Cgd*Cgs*Lg*Ls*Rdson*Vdd + Cgd*Cgs*Ld*Ls*Rdson*Vgg;
  B=Cgd*Lg*Ls*Vdd + Cgd*Ld*Ls*Vgg + Cgs*Lg*Ls*Vdd + Cgs*Ld*Ls*Vgg +
Cgd*Cgs*Ls*Rdson*Rg*Vdd;
  C=Cgd*Lg*Rdson*Vdd + Cgd*Ld*Rdson*Vgg + Cgs*Lg*Rdson*Vdd + Cgs*Ls*Rdson*Vdd +
Cgd*Ls*Rg*Vdd + Cgs*Ls*Rg*Vdd;
  D=Ls*Vdd + Cgd*Rdson*Rg*Vdd + Cgs*Rdson*Rg*Vdd;
  E=Rdson*Vdd;

  %denumerator
  A1=Cgd*Cgs*Ld*Lg*Rdson + Cgd*Cgs*Ld*Ls*Rdson + Cgd*Cgs*Lg*Ls*Rdson;
  B1=Cgd*Ld*Lg + Cgs*Ld*Lg + Cgd*Ld*Ls + Cgs*Ld*Ls + Cgd*Lg*Ls + Cgs*Lg*Ls +
Cgd*Cgs*Ld*Rdson*Rg + Cgd*Cgs*Ls*Rdson*Rg;
  C1=Cgd*Ld*Rdson + Cgd*Ld*Rg + Cgs*Ld*Rg + Cgd*Lg*Rdson + Cgs*Lg*Rdson +
Cgs*Ls*Rdson + Cgd*Ls*Rg + Cgs*Ls*Rg;
  D1=Ld + Ls + Cgd*Rdson*Rg + Cgs*Rdson*Rg;
  E1=Rdson;
  num2=[A B C D E];, den2=[A1 B1 C1 D1 E1];
  Vd=tf(num2,den2);
  fprintf('Vd= '),Vd,fprintf('\n\n')

  %%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %%%% The transfer function for Vs %%%%%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%% W A R N I N G %%%%%%%%%%%%%
  % Ld must have a non zero value for us to get a non zero transfer function
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %numerator
  A=Cgd*Cgs*Lg*Ls*Rdson*Vdd + Cgd*Cgs*Ld*Ls*Rdson*Vgg;
  B=Cgd*Lg*Ls*Vdd + Cgd*Ld*Ls*Vgg + Cgs*Lg*Ls*Vdd + Cgs*Ld*Ls*Vgg +
Cgd*Cgs*Ls*Rdson*Rg*Vdd;
  C=Cgd*Ls*Rg*Vdd + Cgs*Ls*Rg*Vdd + Cgs*Ls*Rdson*Vgg;
  D=Ls*Vdd;
  E=0;

  %denumerator
  A1=Cgd*Cgs*Ld*Lg*Rdson + Cgd*Cgs*Ld*Ls*Rdson + Cgd*Cgs*Lg*Ls*Rdson;
  B1=Cgd*Ld*Lg + Cgs*Ld*Lg + Cgd*Ld*Ls + Cgs*Ld*Ls + Cgd*Lg*Ls + Cgs*Lg*Ls +
Cgd*Cgs*Ld*Rdson*Rg + Cgd*Cgs*Ls*Rdson*Rg;
  C1=Cgd*Ld*Rdson + Cgd*Ld*Rg + Cgs*Ld*Rg + Cgd*Lg*Rdson + Cgs*Lg*Rdson +
Cgs*Ls*Rdson + Cgd*Ls*Rg + Cgs*Ls*Rg;
  D1=Ld + Ls + Cgd*Rdson*Rg + Cgs*Rdson*Rg;
  E1=Rdson;
  num3=[A B C D E];, den3=[A1 B1 C1 D1 E1];
  Vs=tf(num3,den3);
  fprintf('Vs= '),Vs,fprintf('\n\n')

  %%
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%simulation parameters
t=[0:1e-9:1.6e-6];
figure(1)
step(Vg,Vd,Vs),legend ('Vg', 'Vd', 'Vs')
[Vgnume,time]=step(Vg,t);
[Vsnume,time]=step(Vs,t);
[Vdnume,time]=step(Vd,t);
Vds=Vdnume-Vsnume;
Vgs=Vgnume-Vsnume;
Vgd=Vgnume-Vdnume;
figure(2)
plot(t,Vds);,title('Vds')
figure(3)
plot(t,Vgs);,title('Vgs')
figure(4)
plot(t,Vgd);,title('Vgd')
%%
a=0;
t=[0:1e-9:3e-6];
for q=[1:length(t)]
    if q<length(t)/2
        a(q)=0;
    else
        a(q)=1;
    end
end

figure(5)
zavara10=lsim(Vg,a,t);
zavara20=lsim(Vs,a,t);
klom1=zavara10-zavara20;
plot(t,klom1),title('Vgs')

a=0;
t=[0:1e-9:5e-6];
for q=[1:length(t)]
    if q<length(t)/2
        a(q)=1;
    else
        a(q)=0;
    end
end
figure(6)
% zavara1=lsim(Vd,a,t);
% zavara2=lsim(Vs,a,t);
zavara=(Vd-Vs)*input;
klom2(:,i)=lsim(zavara,a,t);
% klom2=zavara1-zavara2;
numericalinput=lsim(input,a,t);
plot(t,klom2(:,i)),title('Vds for different Ls')
xlim([2.49e-006 3.5e-006]);
legend('1e-8','2e-8','3e-8','4e-8','5e-8','6e-8','7e-8','8e-8','9e-8','10e-8');
xlabel('Time (s)');
ylabel('Amplitude (V)')
hold all




% a=0;
% t=[0:1e-9:3e-6];
```

```
   % for q=[1:length(t)]
   %     if q<length(t)/2
   %         a(q)=0;
   %     else
   %         a(q)=1;
   %     end
   % end

   % figure(7)
   % zavara3=lsim(Vg,a,t);
   % zavara4=lsim(Vs,a,t);
   % klom3=zavara3-zavara4;
   % plot(t,klom3),title('Vgs for different Ls')
   % xlim([1.49e-006 2.2e-006]);
   %   legend('1e-8','2e-8','3e-8','4e-8','5e-8','6e-8','7e-8','8e-8','9e-8','10e-
8');
   % xlabel('Time (s)');
   % ylabel('Amplitude (V)')
   % hold all

   % q=1;
   % while t(q)>2.49e-006 &
   %     i=i+1;
   % end
   % j=i
   %
   %
   % i=0;
   % for i=[1:j]
   %     klom2plot(i)=klom2(j-1+i);
   %     tplot(i)=t(i);
   % end


      for k=(1:(3501-2491));

       t1=t';
       tplot(k,1)=t1(2491+k);
       klom2plot(k,i)=klom2(k+2491,i);

   end
   end
   %       xlswrite('D:\matlab       file\experimental       and       modelling
plots\Vds22.xlsx',klom2plot',1,'b2')
   %       xlswrite('D:\matlab       file\experimental       and       modelling
plots\Vds22.xlsx',tplot',1,'A2')
   % xlswrite('D:\written papers\picsVds_Ls2.xlsx',t',1)
```



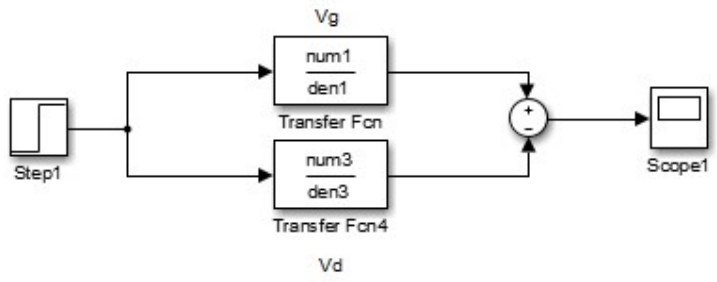
8.2.Dependance of Vgs from Ls

```
clc
clear all
close all

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Setting the symbols
syms Vd Vg Vs s Cgd Cgs Ld Lg Ls Vdd Vgg Cgd Cgs Rg Rdson
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Lgi=[2 4 6 8];
l=length(Lgi);
for i=[1:l]

    Lg=Lgi(i)*1e-9

%Setting the values
Ld=1e-9;  Ls=1000e-9;  Cgs=0.1e-9; Cgd=10e-9;  Rg=22; Vgg=18; Vdd=0;

% Ld=10e-9; Cgs=4e-9; Cgd=2.5e-9; Vgg=0; Vdd=190;
% gfs=1e-3; Vth=5; Rg=22; Rdson=400;Ls=1000e-9;



% Lg=1e-8;
% Ld=1e-9;  Lg=1e-8; Cgs=0.1e-9; Cgd=0.5e-9; Rg=22; Vgg=20; Vdd=0;

%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% The transfer function for Vg %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%numerator
A=Cgd*Cgs*Ld*Lg*Vdd + Cgd*Cgs*Lg*Ls*Vdd + Cgd*Cgs*Ld*Ls*Vgg;
B=Cgd*Cgs*Ld*Rg*Vdd + Cgd*Cgs*Ls*Rg*Vdd;
C=Cgd*Lg*Vdd + Cgd*Ld*Vgg + Cgs*Lg*Vdd + Cgs*Ls*Vgg;
D=Cgd*Rg*Vdd + Cgs*Rg*Vdd;
E=Vgg;

%denumerator
A1=Cgd*Cgs*Ld*Lg + Cgd*Cgs*Ld*Ls + Cgd*Cgs*Lg*Ls;
B1=Cgd*Cgs*Ld*Rg + Cgd*Cgs*Ls*Rg;
C1=Cgd*Ld + Cgd*Lg + Cgs*Lg + Cgs*Ls;
D1=Cgd*Rg + Cgs*Rg;
E1=1;
num1=[A B C D E];, den1=[A1 B1 C1 D1 E1];
Vg=tf(num1,den1);
fprintf('Vg= '),Vg,fprintf('\n\n')
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% The transfer function for Vd %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%% W A R N I N G %%%%%%%%%%%%%
% Ld must have a non zero value for us to get a non zero transfer function
%  Ld=1000e-9;  Ls=1000e-9;  Lg=1000e-9;  Cgs=0.2e-9;  Cgd=1e-12;  Rg=20;  Vgg=20;
Vdd=0;
```

```
% gfs=1e-3; Vth=5; Rdson=1000;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%numerator
A=Cgd*Cgs*Ld*Lg*Vdd + Cgd*Cgs*Lg*Ls*Vdd + Cgd*Cgs*Ld*Ls*Vgg;
B=Cgd*Cgs*Ld*Rg*Vdd + Cgd*Cgs*Ls*Rg*Vdd;
C=Cgd*Lg*Vdd + Cgd*Ld*Vgg + Cgs*Lg*Vdd + Cgs*Ls*Vdd;
D=Cgd*Rg*Vdd + Cgs*Rg*Vdd;
E=Vdd;

%denumerator
A1=Cgd*Cgs*Ld*Lg + Cgd*Cgs*Ld*Ls + Cgd*Cgs*Lg*Ls;
B1=Cgd*Cgs*Ld*Rg + Cgd*Cgs*Ls*Rg;
C1=Cgd*Ld + Cgd*Lg + Cgs*Lg + Cgs*Ls;
D1=Cgd*Rg + Cgs*Rg;
E1=1;
num2=[A B C D E];, den2=[A1 B1 C1 D1 E1];
Vd=tf(num2,den2);
fprintf('Vd= '),Vd,fprintf('\n\n')

%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% The transfer function for Vs %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%% W A R N I N G %%%%%%%%%%%%%
% Ld must have a non zero value for us to get a non zero transfer function
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%numerator
A=Cgd*Cgs*Ld*Lg*Vdd + Cgd*Cgs*Lg*Ls*Vdd + Cgd*Cgs*Ld*Ls*Vgg;
B=Cgd*Cgs*Ld*Rg*Vdd + Cgd*Cgs*Ls*Rg*Vdd;
C=Cgd*Ld*Vdd + Cgd*Lg*Vdd + Cgs*Lg*Vdd + Cgs*Ls*Vgg;
D=Cgd*Rg*Vdd + Cgs*Rg*Vdd;
E=Vdd;

%denumerator
A1=Cgd*Cgs*Ld*Lg + Cgd*Cgs*Ld*Ls + Cgd*Cgs*Lg*Ls;
B1=Cgd*Cgs*Ld*Rg + Cgd*Cgs*Ls*Rg;
C1=Cgd*Ld + Cgd*Lg + Cgs*Lg + Cgs*Ls;
D1=Cgd*Rg + Cgs*Rg;
E1=1;
num3=[A B C D E];, den3=[A1 B1 C1 D1 E1];
Vs=tf(num3,den3);
fprintf('Vs= '),Vs,fprintf('\n\n')

%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%simulation parameters
t=[0:1e-9:1.6e-6];
figure(1)
step(Vg,Vd,Vs),legend ('Vg', 'Vd', 'Vs')
[Vgnume,time]=step(Vg,t);
[Vsnume,time]=step(Vs,t);
[Vdnume,time]=step(Vd,t);
```

```
Vds=Vdnume-Vsnume;
Vgs=Vgnume-Vsnume;
Vgd=Vgnume-Vdnume;
figure(2)
plot(t,Vds);,title('Vds')
figure(3)
plot(t,Vgs);,title('Vgs')
figure(4)
plot(t,Vgd);,title('Vgd')
%%
a=0;
t=[0:1e-9:3e-6];
for q=[1:length(t)]
    if q<length(t)/2
        a(q)=0;
    else
        a(q)=1;
    end
end

figure(5)
zavara10=lsim(Vg,a,t);
zavara20=lsim(Vs,a,t);
klom1=zavara10-zavara20;
plot(t,klom1),title('Vgs')

a=0;
t=[0:0.004e-6:10e-6];
for q=[1:length(t)]
    if q<length(t)/30
        a(q)=0;
    else
        a(q)=1;
    end
end
figure(6)
zavara1=lsim(Vd,a,t);
zavara2=lsim(Vs,a,t);
klom2=zavara1-zavara2;
plot(t,klom2),title('Vds for different Ls')
% xlim([1.49e-006 2.2e-006]);
legend('1e-8','2e-8','3e-8','4e-8','5e-8','6e-8','7e-8','8e-8','9e-8','10e-8');
xlabel('Time (s)');
ylabel('Amplitude (V)')
hold all


figure(7)
zavara3=lsim(Vg,a,t);
zavara4=lsim(Vs,a,t);
klom3(:,i)=zavara3-zavara4;
plot(t,klom3(:,i)),title('Vgs for different Ls')
% xlim([0e-006 5.5e-006]);
legend('10000e-9');
xlabel('Time (s)');
ylabel('Amplitude (V)')
hold all
% xlim([0 2e-006]);



end
while t(i)<5.5e-6
    i=i+1;
```

```
end
j=i


i=0;
for i=[1:j]
    klom3plot(i)=klom3(i);
    tplot(i)=t(i);
end
%       xlswrite('D:\matlab       file\experimental       and       modelling
plots\100ohm.xlsx',klom3plot',1,'C2')
%       xlswrite('D:\matlab       file\experimental       and       modelling
plots\100ohm.xlsx',tplot',1,'A2')

%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%% For Rg=22 ohms%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% while t(i)<2.5e-6
%     i=i+1;
% end
% j=i
%
%
% i=0;
% for i=[1:j]
%     klom3plot(i)=klom3(i);
%     tplot(i)=t(i);
% end
%       xlswrite('D:\matlab       file\experimental       and       modelling
plots\22ohm.xlsx',klom3plot',1,'E2')
%       xlswrite('D:\matlab       file\experimental       and       modelling
plots\22ohm.xlsx',tplot',1,'A2')
```



8.3.Device Modelling transfer functions

```
clc
clear all
close all

% syms Vd Vg Vs s Cgd Cgs Ld Lg Ls Vdd Vgg Cgd Cgs Rg Rdson

Cgs=0.2e-9; Ld=1000e-9; Ls=1000e-9; Lg=1e-9; Rg=100; Vgg=0; Vdd=200; Cgd=1e-11;
gfs=1e-3; Vth=5; Rdson=50;
```

```
  A=Cgd*Lg*Rdson*Vdd+Cgd*Ld*Rdson*Vgg+Cgs*Lg*Rdson*Vdd+Cgs*Ls*Rdson*Vdd-
Cgs*Ls*Rdson*Vgg;
  B=Cgd*Rdson*Rg*Vdd+Cgs*Ls*Rdson*Rg*Vdd;
  C=Rdson*Vdd;

  D=Cgd*Cgs*Ld*Lg*Rdson+Cgd*Cgs*Ld*Ls*Rdson+Cgd*Cgs*Lg*Ls*Rdson;
  E=Cgd*Ld*Lg+Cgs*Ld*Lg+Cgd*Ld*Ls+Cgs*Ld*Ls+Cgd*Lg*Ls+Cgs*Lg*Ls+Cgd*Cgs*Ld*Rdson*
Rg+Cgd*Cgs*Ls*Rdson*Rg;
  F=Cgd*Ld*Rdson+Cgd*Ld*Rg+Cgs*Ld*Rg+Cgd*Lg*Rdson+Cgs*Lg*Rdson+Cgs*Ls*Rdson+Cgd*L
s*Rg+Cgs*Ls*Rg;
  G=Ld+Ls+Cgd*Rdson*Rg+Cgs*Rdson*Rg;
  H=Rdson;


  num=[A B C]; den=[D E F G H];
  transfer=tf(num,den)

  A1=Rg*Cgd; B1=1;
  den1=[A1 B1];
  input=tf(B1,den1)

  new=transfer*input

  a=0;
  t=[0:1e-9:3e-6];
  for i=[1:length(t)]
      if i<length(t)/2
          a(i)=1;
      else
          a(i)=0;
      end
  end
  figure(1)
  zavara1=lsim(transfer,a,t);
  plot(t,zavara1),title('Vds no input')
  xlim([1.5e-006 2.2e-006]);
  legend('0.2e-9');
  xlabel('Time (s)');
  ylabel('Amplitude (V)')
  hold all

  figure(2)
  zavara2=lsim(new,a,t);
  plot(t,zavara2),title('Vds with input')
  xlim([1.5e-006 2.2e-006]);
  legend('0.2e-9');
  xlabel('Time (s)');
  ylabel('Amplitude (V)')
  hold all


  Cgs=0.2e-9; Ld=1000e-9; Ls=1000e-9; Lg=1e-9; Rg=5; Vgg=0; Vdd=200; Cgd=1e-11;
  gfs=1e-3; Vth=5; Rdson=50;

  A=Cgd*Lg*Rdson*Vdd+Cgd*Ld*Rdson*Vgg+Cgs*Lg*Rdson*Vdd+Cgs*Ls*Rdson*Vdd-
Cgs*Ls*Rdson*Vgg;
  B=Cgd*Rdson*Rg*Vdd+Cgs*Ls*Rdson*Rg*Vdd;
  C=Rdson*Vdd;

  D=Cgd*Cgs*Ld*Lg*Rdson+Cgd*Cgs*Ld*Ls*Rdson+Cgd*Cgs*Lg*Ls*Rdson;
  E=Cgd*Ld*Lg+Cgs*Ld*Lg+Cgd*Ld*Ls+Cgs*Ld*Ls+Cgd*Lg*Ls+Cgs*Lg*Ls+Cgd*Cgs*Ld*Rdson*
Rg+Cgd*Cgs*Ls*Rdson*Rg;
```

```
  F=Cgd*Ld*Rdson+Cgd*Ld*Rg+Cgs*Ld*Rg+Cgd*Lg*Rdson+Cgs*Lg*Rdson+Cgs*Ls*Rdson+Cgd*L
s*Rg+Cgs*Ls*Rg;
  G=Ld+Ls+Cgd*Rdson*Rg+Cgs*Rdson*Rg;
  H=Rdson;


  num=[A B C]; den=[D E F G H];
  transfer=tf(num,den)

  A1=Rg*Cgd; B1=1;
  den1=[A1 B1];
  input=tf(B1,den1)

  new=transfer*input

  a=0;
  t=[0:1e-9:3e-6];
  for i=[1:length(t)]
      if i<length(t)/2
          a(i)=1;
      else
          a(i)=0;
      end
  end
  figure(1)
  zavara1=lsim(transfer,a,t);
  plot(t,zavara1),title('Vds no input')
  xlim([1.5e-006 2.2e-006]);
  legend('0.2e-9');
  xlabel('Time (s)');
  ylabel('Amplitude (V)')
  hold all

  figure(2)
  zavara2=lsim(new,a,t);
  plot(t,zavara2),title('Vds with input')
  xlim([1.5e-006 2.2e-006]);
  legend('0.2e-9');
  xlabel('Time (s)');
  ylabel('Amplitude (V)')
  hold all
```

8.4.Device modelling solving equations

t0-t1

```
clc
clear all
close all
%
% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Setting the symbols
syms Vd Vg Vs s Cgd Cgs Ld Lg Ls Vdd Vgg Cgd Cgs Rg Rdson
A='0=(Vd-Vg)*s*Cgd+((Vd-Vdd)/(s*Ld))';
B='0=((Vg-Vgg)/(Rg+s*Lg))+(Vg-Vs)*s*Cgs+(Vg-Vd)*s*Cgd';
C='0=(Vs-Vg)*s*Cgs+((Vs-Vdd)/(s*Ls))';
[Vd Vg Vs]=solve(A,B,C,Vd,Vg,Vs);
% collect(Vs)

% fprintf('Vs=')
% Vs
% fprintf('\n\n\n')
```

```
%
% fprintf('Vg=')
% Vg
% fprintf('\n\n\n')
%
% fprintf('Vd=')
% Vd

giouria=Vg-Vs;
pretty(collect(giouria))
```

t1-t2

```
clc
clear all
close all
%
% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Setting the symbols
syms Vd Vg Vs s Cgd Cgs Ld Lg Ls Vdd Vgg Cgd Cgs Rg Rdson
A='0=(Vd-Vg)*s*Cgd+((Vd-Vdd)/(s*Ld))+((Vd-Vs)/(gfs*(Vgs-Vth)))';
B='0=((Vg-Vgg)/(Rg+s*Lg))+(Vg-Vs)*s*Cgs+(Vg-Vd)*s*Cgd';
C='0=(Vs-Vg)*s*Cgs+((Vs-Vd)/(gfs*(Vgs-Vth)))+(Vs/(s*Ls))';
[Vd, Vg, Vs]=solve(A,B,C,Vd,Vg,Vs);
% collect(Vs)

fprintf('Vs=')
pretty(collect(Vs))
fprintf('\n\n\n')

fprintf('Vg=')
pretty(collect(Vg))
fprintf('\n\n\n')

fprintf('Vd=')
pretty(collect(Vd))

% giouria=Vd-Vs;
% pretty(collect(giouria))
```

t2-t4

```
clc
clear all
close all
%
% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Setting the symbols
syms Vd Vg Vs s Cgd Cgs Ld Lg Ls Vdd Vgg Cgd Cgs Rg Rdson
A='0=(Vd-Vg)*s*Cgd+((Vd-Vdd)/(s*Ld))+((Vd-Vs)/Rdson)';
B='0=((Vg-Vgg)/(Rg+s*Lg))+(Vg-Vs)*s*Cgs+(Vg-Vd)*s*Cgd';
C='0=(Vs-Vg)*s*Cgs+((Vs-Vd)/Rdson)+(Vs/(s*Ls))';
[Vd Vg Vs]=solve(A,B,C,Vd,Vg,Vs);
% collect(Vs)

pretty(collect(Vs))
fprintf('\n\n\n')
pretty(collect(Vg))
fprintf('\n\n\n')
pretty(collect(Vd))
```

```
fprintf('\n\n\n')
giouria=Vd-Vs;
pretty(collect(giouria))
```

8.5.Varying Rdson resistance

```
clc
clear all
close all

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Setting the symbols
syms Vd Vg Vs s Cgd Cgs Ld Lg Ls Vdd Vgg Cgd Cgs Rg Rdson
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Rdsoni=[3000];
l=length(Rdsoni);
for i=[1:l]

    Rdson=Rdsoni(i);

%Setting the values
% Ld=1e-9;  Lg=1e-8; Cgs=0.1e-9; Cgd=10e-9;  Rg=22; Vgg=0; Vdd=200;
%  Rdson=200;
% % % % % %  Ld=1e-10; Lg=1e-10; Cgs=0.7e-10; Cgd=1e-11; Vgg=1; Vdd=200;
% % % % % % gfs=1e-3; Vth=5; Ls=30e-6;Rg=22;
Ld=10e-9; Lg=10e-9; Cgs=50e-11; Cgd=3e-9; Vgg=0; Vdd=190;
gfs=1e-3; Vth=5; Rg=100; Ls=2e-6;
% Ld=1e-12; Ls=1000e-12; Lg=1e-12; Cgs=0.6e-12; Cgd=1e-13; Rg=20e-3; Vgg=20;
Vdd=200;
% gfs=1e-3; Vth=5; Rdson=10e-3;
%%
numinput=[0 1];
deninput=[Rg*Cgd 1];
input=tf(numinput,deninput);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% The transfer function for Vg %%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%numerator
A=Cgd*Cgs*Lg*Ls*Rdson*Vdd + Cgd*Cgs*Ld*Ls*Rdson*Vgg;
B=Cgd*Lg*Ls*Vdd + Cgd*Ld*Ls*Vgg + Cgs*Lg*Ls*Vdd + Cgs*Ld*Ls*Vgg +
Cgd*Cgs*Ls*Rdson*Rg*Vdd;
C=Cgd*Lg*Rdson*Vdd + Cgd*Ld*Rdson*Vgg + Cgd*Ls*Rg*Vdd + Cgs*Ls*Rg*Vdd +
Cgs*Ls*Rdson*Vgg;
D=Ld*Vgg + Ls*Vgg + Cgd*Rdson*Rg*Vdd;
E=Rdson*Vgg;

%denumerator
A1=Cgd*Cgs*Ld*Lg*Rdson + Cgd*Cgs*Ld*Ls*Rdson + Cgd*Cgs*Lg*Ls*Rdson;
B1=Cgd*Ld*Lg + Cgs*Ld*Lg + Cgd*Ld*Ls + Cgs*Ld*Ls + Cgd*Lg*Ls + Cgs*Lg*Ls +
Cgd*Cgs*Ld*Rdson*Rg + Cgd*Cgs*Ls*Rdson*Rg;
C1=Cgd*Ld*Rdson + Cgd*Ld*Rg + Cgs*Ld*Rg + Cgd*Lg*Rdson + Cgs*Lg*Rdson +
Cgs*Ls*Rdson + Cgd*Ls*Rg + Cgs*Ls*Rg;
D1=Ld + Ls + Cgd*Rdson*Rg + Cgs*Rdson*Rg;
```

```
  E1=Rdson;
  num1=[A B C D E];, den1=[A1 B1 C1 D1 E1];
  Vg=tf(num1,den1);
  fprintf('Vg= '),Vg,fprintf('\n\n')
  %%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %%%% The transfer function for Vd %%%%%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%% W A R N I N G %%%%%%%%%%%%%
  % Ld must have a non zero value for us to get a non zero transfer function
  %  Ld=1000e-9;  Ls=1000e-9;  Lg=1000e-9;  Cgs=0.2e-9;  Cgd=1e-12;  Rg=20;  Vgg=20;
Vdd=0;
  % gfs=1e-3; Vth=5; Rdson=1000;
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %numerator
  A=Cgd*Cgs*Lg*Ls*Rdson*Vdd + Cgd*Cgs*Ld*Ls*Rdson*Vgg;
  B=Cgd*Lg*Ls*Vdd   +   Cgd*Ld*Ls*Vgg   +   Cgs*Lg*Ls*Vdd   +   Cgs*Ld*Ls*Vgg   +
Cgd*Cgs*Ls*Rdson*Rg*Vdd;
  C=Cgd*Lg*Rdson*Vdd + Cgd*Ld*Rdson*Vgg + Cgs*Lg*Rdson*Vdd + Cgs*Ls*Rdson*Vdd +
Cgd*Ls*Rg*Vdd + Cgs*Ls*Rg*Vdd;
  D=Ls*Vdd + Cgd*Rdson*Rg*Vdd + Cgs*Rdson*Rg*Vdd;
  E=Rdson*Vdd;

  %denumerator
  A1=Cgd*Cgs*Ld*Lg*Rdson + Cgd*Cgs*Ld*Ls*Rdson + Cgd*Cgs*Lg*Ls*Rdson;
  B1=Cgd*Ld*Lg + Cgs*Ld*Lg + Cgd*Ld*Ls + Cgs*Ld*Ls + Cgd*Lg*Ls + Cgs*Lg*Ls +
Cgd*Cgs*Ld*Rdson*Rg + Cgd*Cgs*Ls*Rdson*Rg;
  C1=Cgd*Ld*Rdson  +  Cgd*Ld*Rg  +  Cgs*Ld*Rg  +  Cgd*Lg*Rdson  +  Cgs*Lg*Rdson  +
Cgs*Ls*Rdson + Cgd*Ls*Rg + Cgs*Ls*Rg;
  D1=Ld + Ls + Cgd*Rdson*Rg + Cgs*Rdson*Rg;
  E1=Rdson;
  num2=[A B C D E];, den2=[A1 B1 C1 D1 E1];
  Vd=tf(num2,den2);
  fprintf('Vd= '),Vd,fprintf('\n\n')

  %%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %%%% The transfer function for Vs %%%%%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%% W A R N I N G %%%%%%%%%%%%%
  % Ld must have a non zero value for us to get a non zero transfer function
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

  %numerator
  A=Cgd*Cgs*Lg*Ls*Rdson*Vdd + Cgd*Cgs*Ld*Ls*Rdson*Vgg;
  B=Cgd*Lg*Ls*Vdd   +   Cgd*Ld*Ls*Vgg   +   Cgs*Lg*Ls*Vdd   +   Cgs*Ld*Ls*Vgg   +
Cgd*Cgs*Ls*Rdson*Rg*Vdd;
  C=Cgd*Ls*Rg*Vdd + Cgs*Ls*Rg*Vdd + Cgs*Ls*Rdson*Vgg;
  D=Ls*Vdd;
  E=0;
```

```
  %denumerator
  A1=Cgd*Cgs*Ld*Lg*Rdson + Cgd*Cgs*Ld*Ls*Rdson + Cgd*Cgs*Lg*Ls*Rdson;
  B1=Cgd*Ld*Lg  +  Cgs*Ld*Lg  +  Cgd*Ld*Ls  +  Cgs*Ld*Ls  +  Cgd*Lg*Ls  +  Cgs*Lg*Ls  +
Cgd*Cgs*Ld*Rdson*Rg + Cgd*Cgs*Ls*Rdson*Rg;
  C1=Cgd*Ld*Rdson  +  Cgd*Ld*Rg  +  Cgs*Ld*Rg  +  Cgd*Lg*Rdson  +  Cgs*Lg*Rdson  +
Cgs*Ls*Rdson + Cgd*Ls*Rg + Cgs*Ls*Rg;
  D1=Ld + Ls + Cgd*Rdson*Rg + Cgs*Rdson*Rg;
  E1=Rdson;
  num3=[A B C D E];, den3=[A1 B1 C1 D1 E1];
  Vs=tf(num3,den3);
  fprintf('Vs= '),Vs,fprintf('\n\n')

  %%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %simulation parameters
  t=[0:1e-9:1.6e-6];
  figure(1)
  step(Vg,Vd,Vs),legend ('Vg', 'Vd', 'Vs')
  [Vgnume,time]=step(Vg,t);
  [Vsnume,time]=step(Vs,t);
  [Vdnume,time]=step(Vd,t);
  Vds=Vdnume-Vsnume;
  Vgs=Vgnume-Vsnume;
  Vgd=Vgnume-Vdnume;
  figure(2)
  plot(t,Vds);,title('Vds')
  figure(3)
  plot(t,Vgs);,title('Vgs')
  figure(4)
  plot(t,Vgd);,title('Vgd')
  %%
  a=0;
  t=[0:1e-9:3e-6];
  for q=[1:length(t)]
      if q<length(t)/2
          a(q)=0;
      else
          a(q)=1;
      end
  end

  figure(5)
  zavara10=lsim(Vg,a,t);
  zavara20=lsim(Vs,a,t);
  klom1=zavara10-zavara20;
  plot(t,klom1),title('Vgs')

  a=0;
  t=[0:1e-9:5e-6];
  for q=[1:length(t)]
      if q<length(t)/2
          a(q)=1;
      else
          a(q)=0;
      end
  end
  figure(6)
  % zavara1=lsim(Vd,a,t);
  % zavara2=lsim(Vs,a,t);
  zavara=(Vd-Vs)*input;
  klom2=lsim(zavara,a,t);
  % klom2=zavara1-zavara2;
```

```
numericalinput=lsim(input,a,t);
plot(t,klom2),title('Vds for different Ls')
xlim([2.4995e-006 4e-006]);
legend('1e-8','2e-8','3e-8','4e-8','5e-8','6e-8','7e-8','8e-8','9e-8','10e-8');
xlabel('Time (s)');
ylabel('Amplitude (V)')
hold all




% a=0;
% t=[0:1e-9:3e-6];
% for q=[1:length(t)]
%     if q<length(t)/2
%         a(q)=0;
%     else
%         a(q)=1;
%     end
% end

% figure(7)
% zavara3=lsim(Vg,a,t);
% zavara4=lsim(Vs,a,t);
% klom3=zavara3-zavara4;
% plot(t,klom3),title('Vgs for different Ls')
% xlim([1.49e-006 2.2e-006]);
%   legend('1e-8','2e-8','3e-8','4e-8','5e-8','6e-8','7e-8','8e-8','9e-8','10e-
8');
% xlabel('Time (s)');
% ylabel('Amplitude (V)')
% hold all


while t(i)<2.5e-6
    i=i+1;
end
j=i


i=0;
for i=[1:j]
    klom2plot(i)=klom2(j-1+i);
    tplot(i)=t(i);
end

end


%       xlswrite('D:\matlab       file\experimental       and       modelling
plots\Vds100.xlsx',klom2plot',1,'B2')
%       xlswrite('D:\matlab       file\experimental       and       modelling
plots\Vds100.xlsx',tplot',1,'A2')
```

8.6.Voltage and current for Diode

```
clear all
close all
```

```
clc

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

                                  %%%%%%%
                                  %DIODE%
                                  %%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Setting the symbols
% syms Rs Rak C Lstray s t
% for i=[1:2:10]

%%
Lstrayi=[ 0.3 ];
l=length(Lstrayi);
for i=[1:l]

   Lstray=Lstrayi(i)*1e-9;
%Input delay
Cgd=0.7e-9;
Rg=100;
numinput=[0 1];
deninput=[Rg*Cgd 1];
input=tf(numinput,deninput);
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Rs=30e-3; Rak=1; C=11e-9; Lstray=55e-9; Vstep=200;
Rs=4e-4;  C=50e-8;
Rak=1e-5;
% t=linspace(0,2e-6,700);
% t=(0:0.1e-6:200e-6);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% setting up the decay rate 'a' the damping factor 'zita' and the undamped
% natural frequency 'omega'

a=(Rs*Rak*C+Lstray)/(2*Rak*Lstray*C);
omega=sqrt((Rs+Rak)/(Rak*Lstray*C));
zita=a/omega;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Voltage output for diode using transfer function

A=1;
B=2*zita*omega;
D=omega^2;
E=0;
den= [A B D ];
num= [0 0 omega^2];
sys1=tf(num,den);
sys=sys1*input;

t=[0:1e-9:10e-6];
lengthtime=length(t)/2;

for i=[1:length(t)]
    if i<lengthtime
```

```
            u(i)=0;
        else
            u(i)=190;
        end
    end
    figure (1)
    V=lsim(sys,u,t);
    plot(t,V)
    hold all
    title('Diode voltage responce with input delay')
    xlabel('Time (µs)')
    ylabel ('Amplitude (V)')
    hold all

    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %Transfer function for I

    numZ=[0 0 omega^2];
    denZ=[A B D ];
    Z=tf(numZ,denZ)
    sysI=Z*input;

    for i=[1:length(t)]
        if i<lengthtime
            u(i)=63;
        else
            u(i)=3;
        end
    end
    % [u,t]=gensig('square',1e-6,2e-6,3e-10);
    % u=u*60;

    Iinv=lsim(sysI,u,t);
    figure (2)
    plot(t,Iinv)
    title('Diode current responce with input delay')
    xlabel('Time (µs)')
    ylabel ('Amplitude (A)')
    hold all
    % end

    end
    i=1;
    while t(i)<5e-6
        i=i+1;
    end
    j=i
    i=1;
    while t(i)<7e-6
        i=i+1;
    end
    k=i;

    for i=[1:k-j]
        tplot(i)=t(j+i);
        Iinvplot(i)=Iinv(j+i);
        Vplot(i)=V(j+i);
    end
    %  xlswrite('D:\matlab  file\experimental  and  modelling  plots\Vak22.xlsx',
Vplot',1,'B2')
    % xlswrite('D:\matlab file\experimental and modelling plots\Vak_Iak100.xlsx',
Iinvplot',1,'F2')
    % xlswrite('D:\matlab file\experimental and modelling plots\Vak_Iak100.xlsx',
tplot',1,'A2')
```

```
  % xlswrite('D:\matlab file\experimental and modelling plots\Vak_Iak100.xlsx',
Vplot',1,'B2')
```

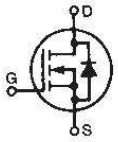
IXYS Advanced Technical Information

HiPerFET™ Power MOSFETs

IXFK 20N120
IXFX 20N120

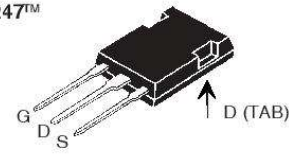
V_{DSS} = 1200 V
I_{D25} = 20 A
$R_{DS(on)}$ = 0.75 Ω

$t_{rr} \leq 300$ ns

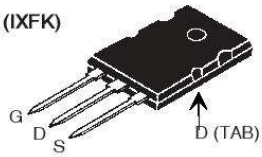


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1200	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	1200	V
V_{GS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C	20	A
I_{DM}	T_C = 25°C, Note 1	80	A
I_{AR}	T_C = 25°C	10	A
E_{AR}	T_C = 25°C	40	mJ
E_{AS}	T_C = 25°C	2	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$ $T_J \leq$ 150°C, R_G = 2 Ω	5	V/ns
P_D	T_C = 25°C	780	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.063 in.) from case for 10 s	300	°C
M_d	Mounting torque TO-264	0.9/6	Nm/lb.in.
Weight	PLUS 247	6	g
	TO-264	10	g

PLUS247™ (IXFX)



TO-264 AA (IXFK)



G = Gate D = Drain
S = Source TAB = Drain

Features
- International standard packages
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic rectifier

Applications
- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls

Advantages
- PLUS 247™ package for clip or spring mounting
- Space savings
- High power density

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 1mA		1200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA		2.5		4.5	V
I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$ V_{GS} = 0 V	T_J = 25°C T_J = 125°C			100 2	µA mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \bullet I_{D25}$ Note 2				0.75	Ω

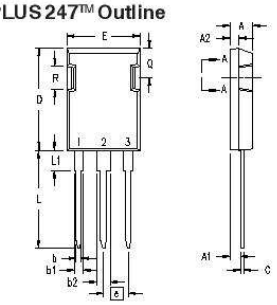
Symbol	Test Conditions (T$_J$ = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 • I_{D25} Note 2	15	27		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		7400		pF
C_{oss}			550		pF
C_{rss}			100		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25} R_G = 1 Ω (External),		25		ns
t_r			45		ns
$t_{d(off)}$			75		ns
t_f			20		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		160		nC
Q_{gs}			35		nC
Q_{gd}			60		nC
R_{thJC}				0.16	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions (T$_J$ = 25°C, unless otherwise specified)	min.	typ.	max.	
I_S	V_{GS} = 0 V			20	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			80	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	$I_F = I_S$, -di/dt = 100 A/µs, V_R = 100 V			300	ns
Q_{RM}			1.4		µC
I_{RM}			8		A

Note: 1. Pulse width limited by T_{JM}
2. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %

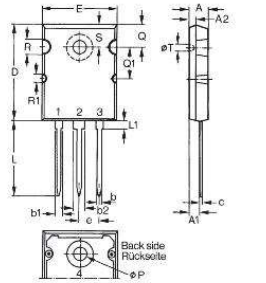
PLUS 247™ Outline



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)
4 - Drain (Collector)

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

TO-264 AA Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46BSC		.215BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

Fig. 1. Output Characteristics @ 25 deg. C

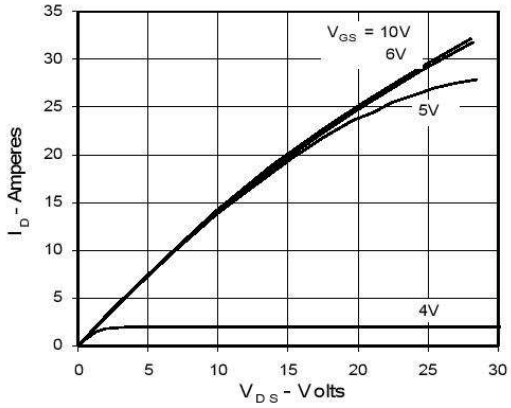


Fig. 2. Output Characteristics @ 125 Deg. C

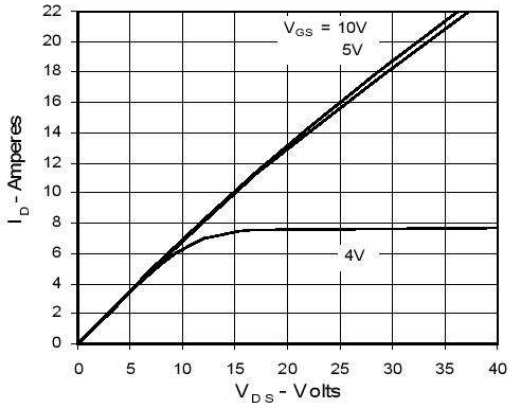


Fig. 3. $R_{DS(on)}$ Normalized to I_{D25} Value vs. Junction Temperature

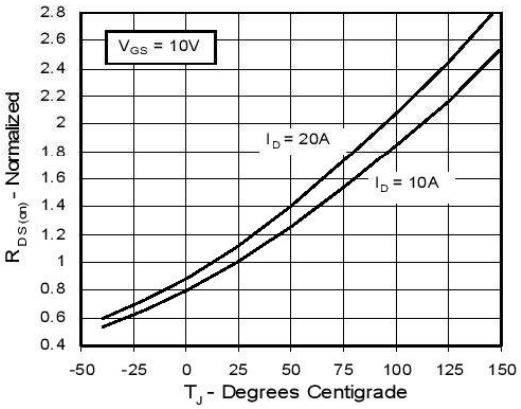


Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D

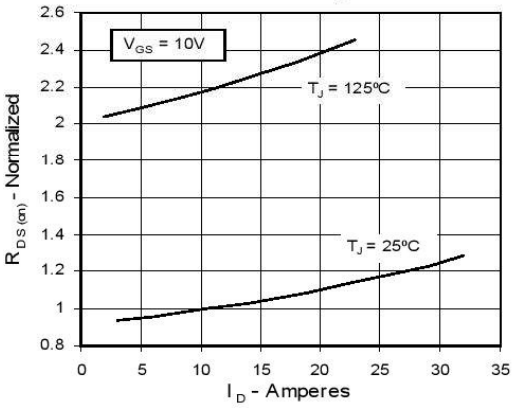


Fig. 5. Drain Current vs. Case Temperature

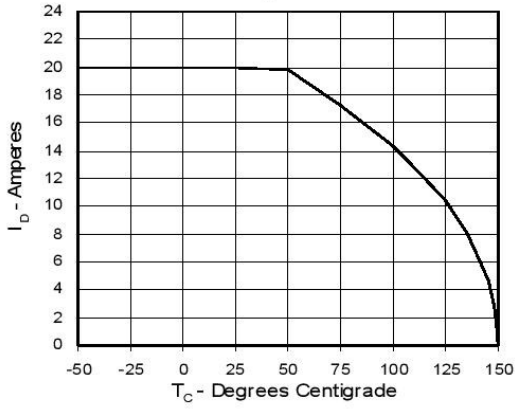


Fig. 6. Input Admittance

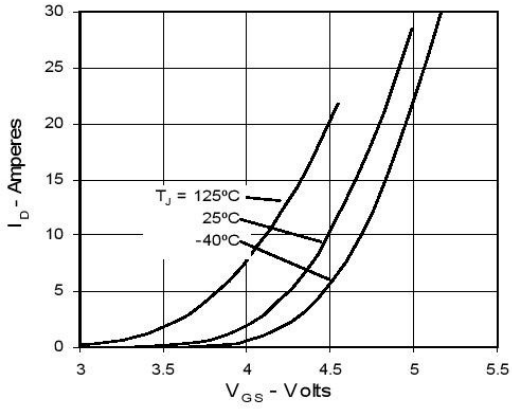


Fig. 7. Transconductance

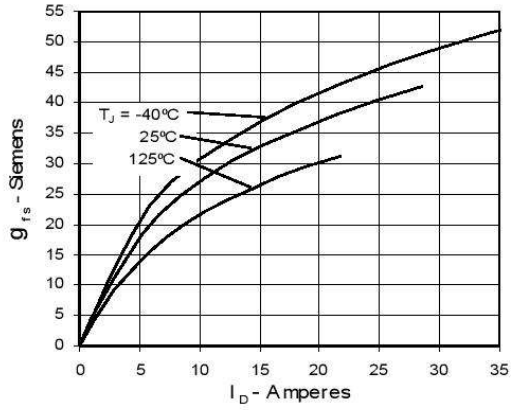


Fig. 8. Source Current vs. Source-To-Drain Voltage

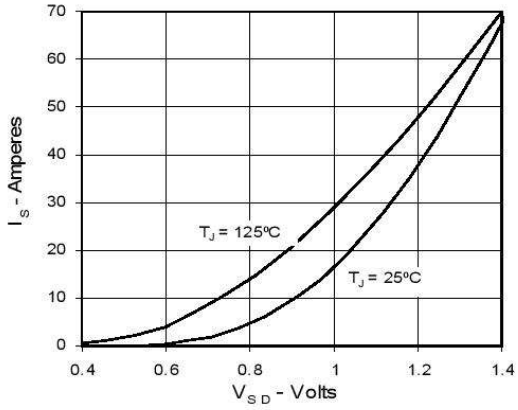


Fig. 9. Gate Charge

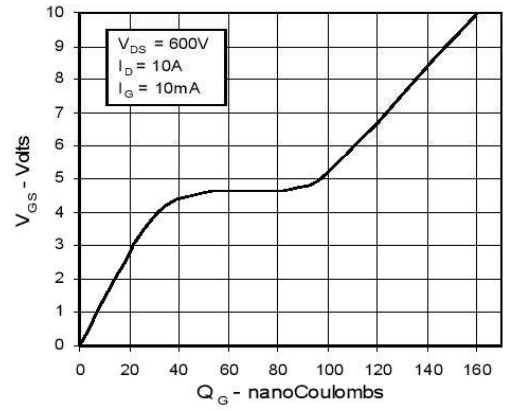


Fig. 10. Capacitance

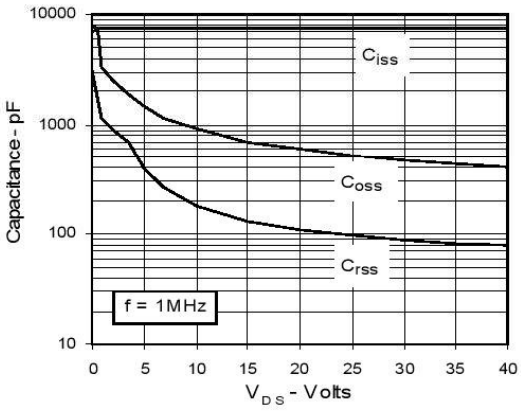
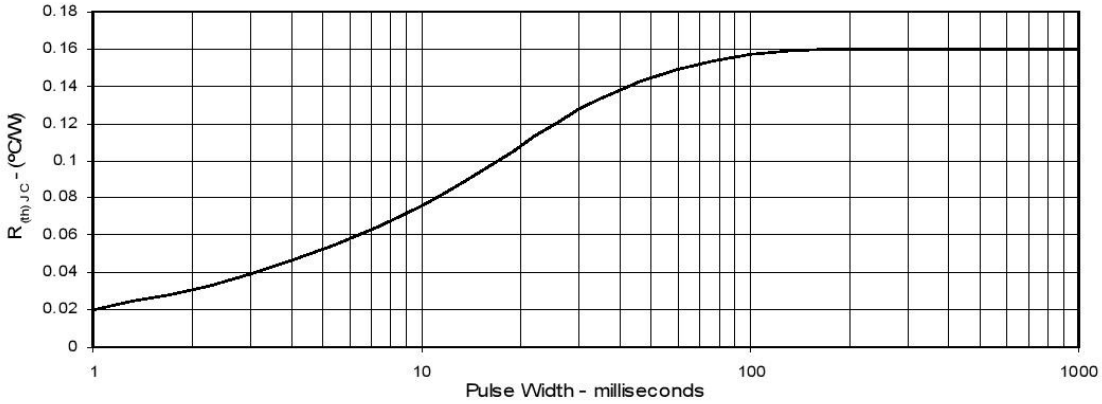


Fig. 11. Maximum Transient Thermal Resistance



CMF10120D-Silicon Carbide Power MOSFET

Z-FET™ MOSFET

N-Channel Enhancement Mode

V_{DS}	= 1200 V
$I_{D(MAX)}$	= 24 A
$R_{DS(on)}$	= 160mΩ

Features

- High Speed Switching with Low Capacitances
- High Blocking Voltage with Low $R_{DS(on)}$
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased System Switching Frequency

Applications

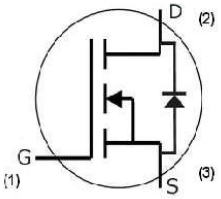
- Solar Inverters
- High Voltage DC/DC Converters
- Motor Drives
- Switch Mode Power Supplies

Package

TO-247-3

Halogen-Free

RoHS COMPLIANT



Part Number	Package
CMF10120D	TO-247-3

Maximum Ratings (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
I_D	Continuous Drain Current	24	A	V_{GS}@20V, T_C = 25°C	Fig. 10
		13		V_{GS}@20V, T_C = 100°C	
I_{Dpulse}	Pulsed Drain Current	49	A	Pulse width t_P limited by T_{jmax} T_C = 25°C	
E_{AS}	Single Pulse Avalanche Energy	1.2	J	I_D = 10A, V_{DD} = 50 V, L = 20 mH t_{AR} limited by T_{jmax}	Fig. 15
E_{AR}	Repetitive Avalanche Energy	0.8	J		
I_{AR}	Repetitive Avalanche Current	10	A	I_D = 10A, V_{DD} = 50 V, L = 15 mH t_{AR} limited by T_{jmax}	
V_{GS}	Gate Source Voltage	-5/+25	V		
P_{tot}	Power Dissipation	134	W	T_C=25°C	Fig. 9
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +135	°C		
T_L	Solder Temperature	260	°C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0V, I_D = 50μA	
$V_{GS(th)}$	Gate Threshold Voltage		2.4	3.5	V	V_{DS} = V_{GS}, I_D = 0.5 mA	Fig. 11
			3.1	4.1		V_{DS} = V_{GS}, I_D = 1.0 mA	
			1.8		V	V_{DS} = V_{GS}, I_D = 0.5 mA, T_J = 135°C	
			2.3		V	V_{DS} = V_{GS}, I_D = 1.0 mA, T_J = 135°C	
I_{DSS}	Zero Gate Voltage Drain Current		0.5	50	μA	V_{DS} = 1200V, V_{GS} = 0V	
			5	150		V_{DS} = 1200V, V_{GS} = 0V, T_J = 135°C	
I_{GSS}	Gate-Source Leakage Current			0.25	μA	V_{GS} = 20V, V_{DS} = 0V	
$R_{DS(on)}$	Drain-Source On-State Resistance		160	200	mΩ	V_{GS} = 20V, I_D = 10A	Fig. 3
			190	240		V_{GS} = 20V, I_D = 10A, T_J = 135°C	
g_{fs}	Transconductance		4.2		S	V_{DS}= 20V, I_{DS}= 10A	Fig. 6
			3.9			V_{DS}= 20V, I_{DS}= 10A, T_J = 135°C	
C_{iss}	Input Capacitance		928		pF	V_{GS} = 0V V_{DS} = 800V f = 1MHz V_{AC} = 25mV	Fig. 13
C_{oss}	Output Capacitance		63				
C_{rss}	Reverse Transfer Capacitance		7.5				
E_{oss}	C_{oss} Stored Energy		32		μJ		Fig 14
$t_{d(on)v}$	Turn-On Delay Time		8.8		ns	V_{DD} = 800V, V_{GS} = 0/20V I_D = 10A $R_{G(ext)}$ = 2.5Ω, R_L = 40Ω Timing relative to V_{DS}	fig. 17
t_{fv}	Fall Time		21				
$t_{d(off)V}$	Turn-Off Delay Time		38				
t_{rV}	Rise Time		34				
R_G	Internal Gate Resistance		13.6		Ω	f = 1MHz, V_{AC} = 25mV	

Built-in SiC Body Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.5		V	V_{GS} = -5V, I_F=5A, T_J = 25°C	
		3.1			V_{GS} = -2V, I_F=5A, T_J = 25°C	
t_{rr}	Reverse Recovery Time	138		ns	V_{GS} = -5V, I_F=10A, T_J = 25°C V_R = 800V, di_F/dt= 100A/μs	Fig. 22
Q_{rr}	Reverse Recovery Charge	94		nC		
I_{rrm}	Peak Reverse Recovery Current	1.57		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.66	0.82	K/W		Fig. 7
$R_{\theta CS}$	Case to Sink, w/ Thermal Compound	0.25				
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient		40			

Gate Charge Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
Q_{gs}	Gate to Source Charge	11.8		nC	V_{DD} = 800V, V_{GS} = 0/20V I_D =10A Per JEDEC24 pg 27	Fig.12
Q_{gd}	Gate to Drain Charge	21.5				
Q_g	Gate Charge Total	47.1				

Typical Performance

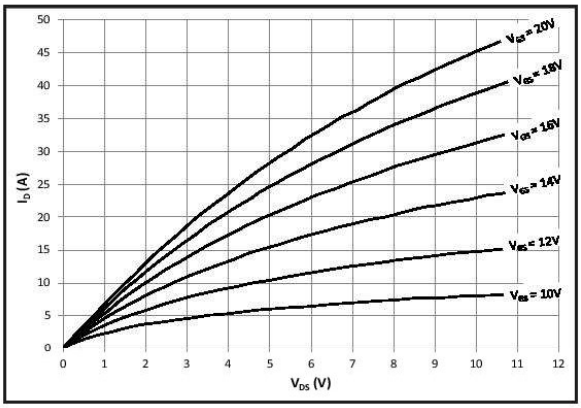


Figure 1. Typical Output Characteristics T_J = 25ºC

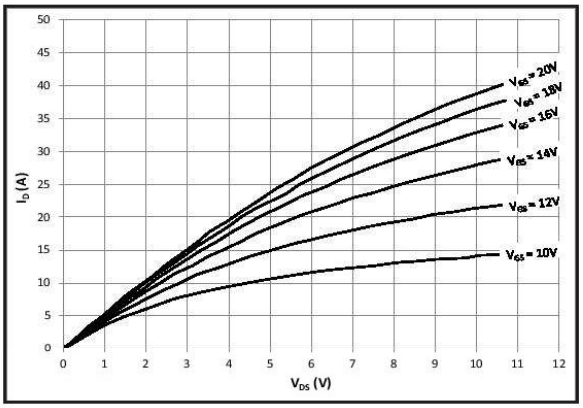


Figure 2. Typical Output Characteristics T_J = 135ºC

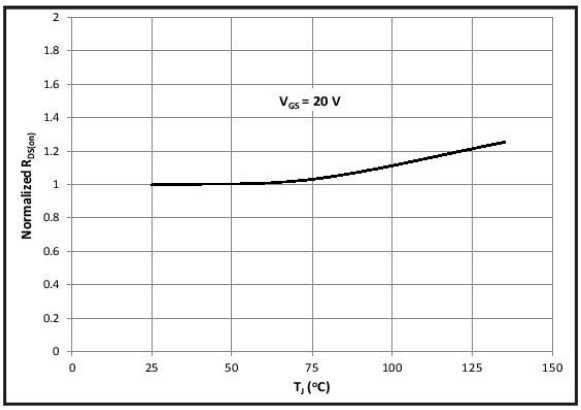


Figure 3. Normalized On-Resistance vs. Temperature

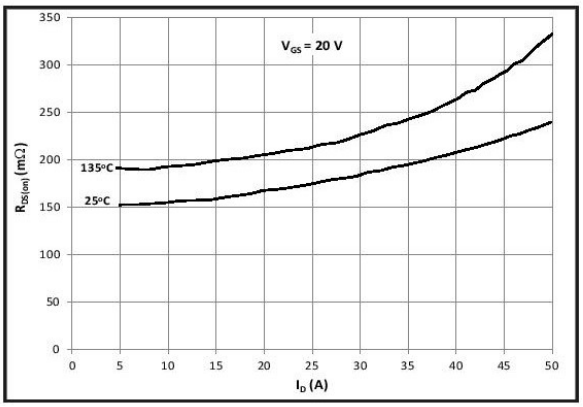


Figure 4. On-Resistance vs. Drain Current

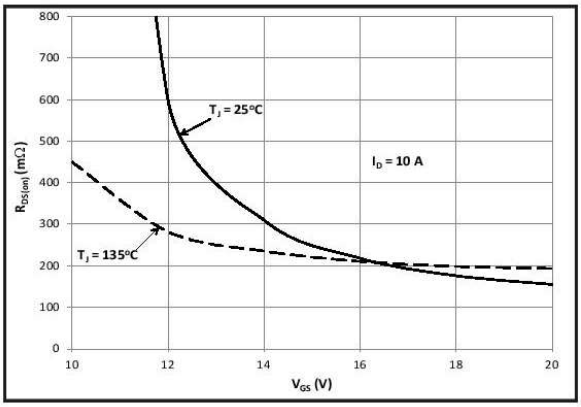


Figure 5. On-Resistance vs. Gate Voltage

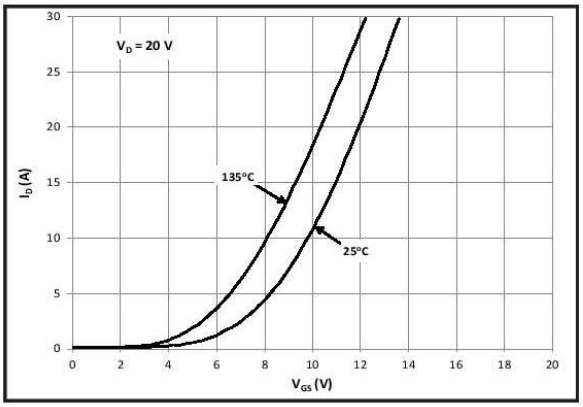


Figure 6. Typical Transfer Characteristics

Typical Performance

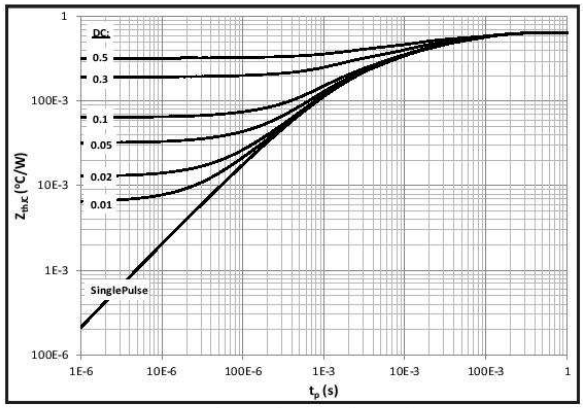


Figure 7. Transient Thermal Impedance (Junction - Case) with Duty Cycle

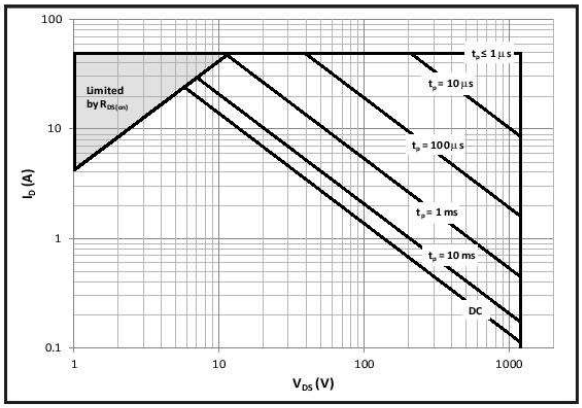


Figure 8. Safe Operating Area

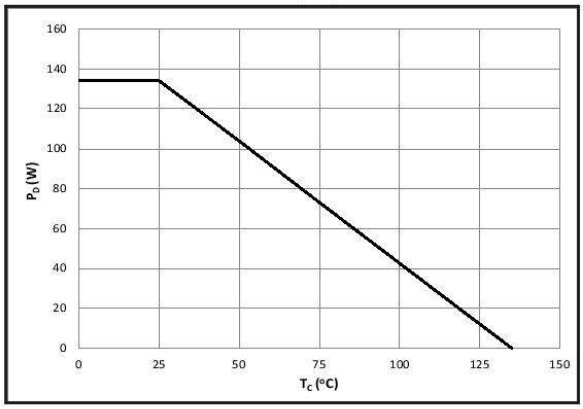


Figure 9. Power Dissipation Derating Curve

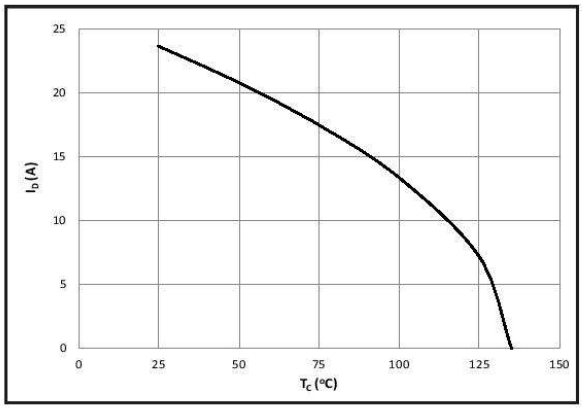


Figure 10. Continuous Current Derating Curve

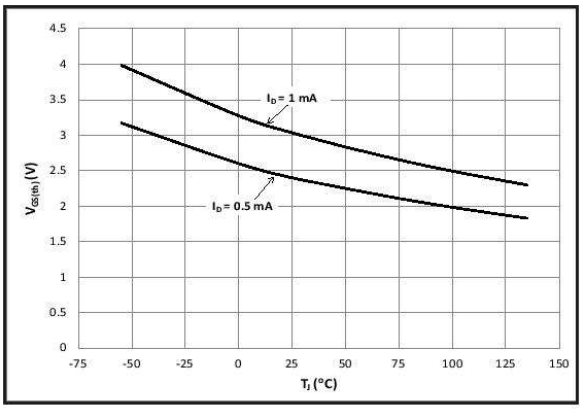


Figure 11. Gate Threshold Voltage vs. Temperature

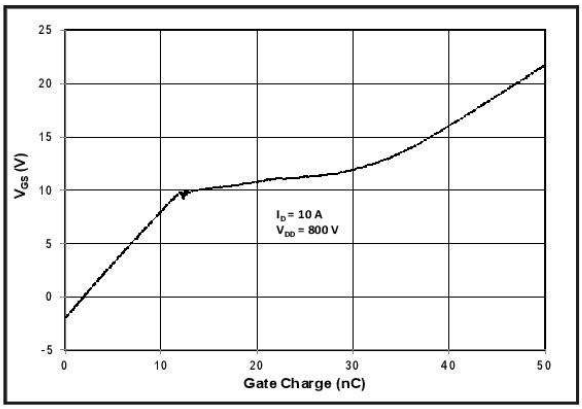
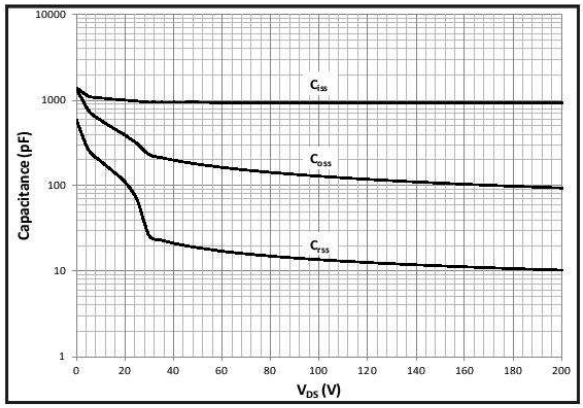


Figure 12. Typical Gate Charge Characteristics (25°C)

Typical Performance



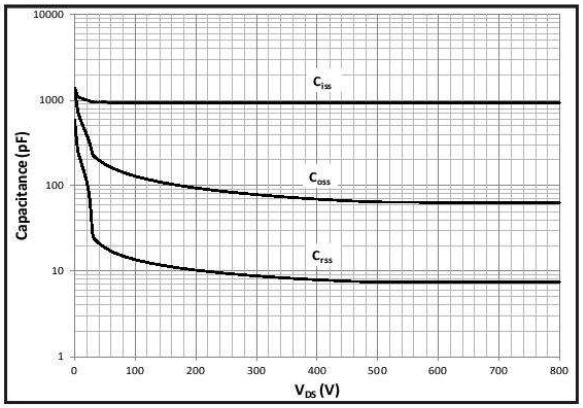


Figure 13A and 13B. Typical Capacitances vs. Drain Voltage at V_{GS} = 0V and f = 1 MHz

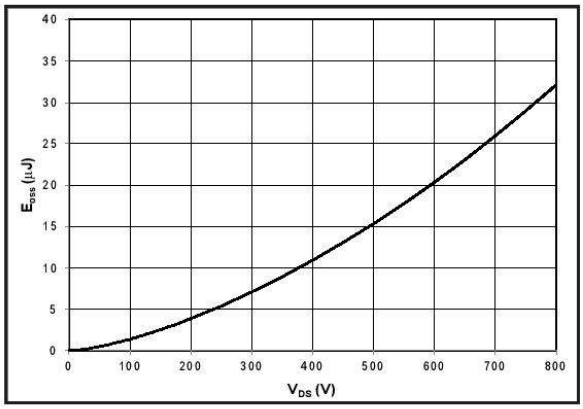


Figure 14. Typical C_{OSS} Stored Energy

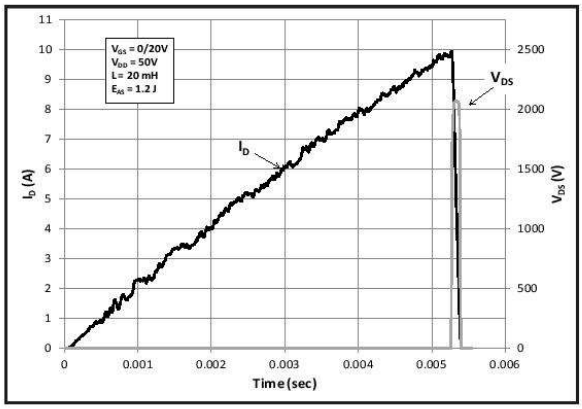


Figure 15. Typical Unclamped Inductive Switching Waveforms Showing Avalanche Capability

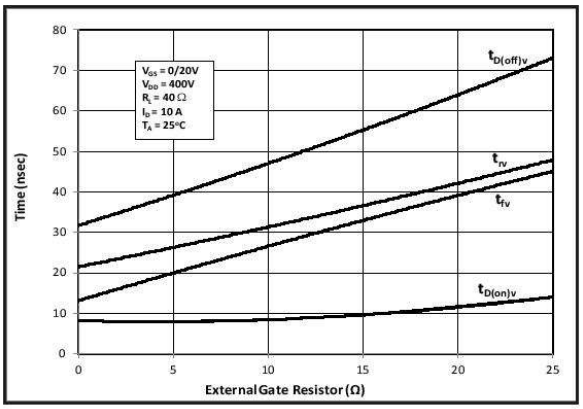


Figure 16. Resistive Switching Times vs. External R_G at V_{DD} = 400V, I_D = 10A

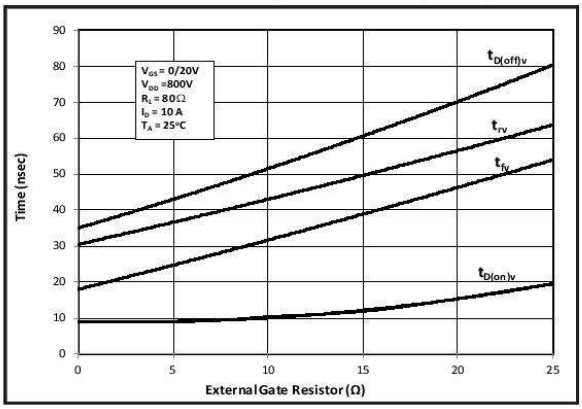


Figure 17. Resistive Switching Times vs. External R_G at V_{DD} = 800V, I_D = 10A

Typical Performance

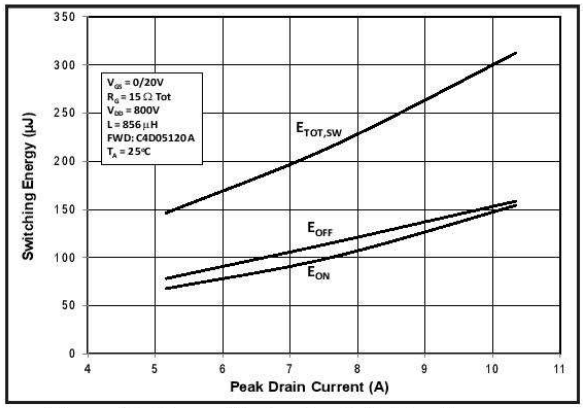


Figure 18. Clamped Inductive Switching Energy vs. Drain Current (Fig. 20)

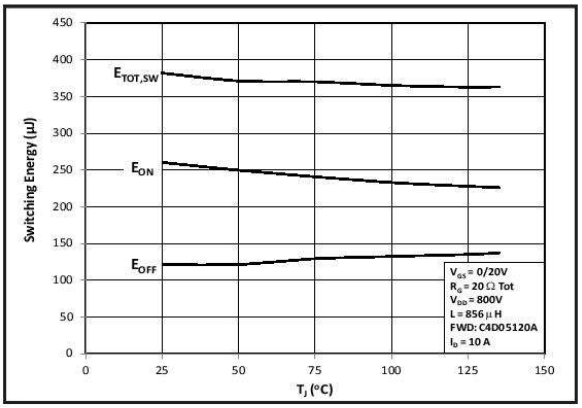


Figure 19. Clamped Inductive Switching Energy vs. Junction Temperature (Fig 20)

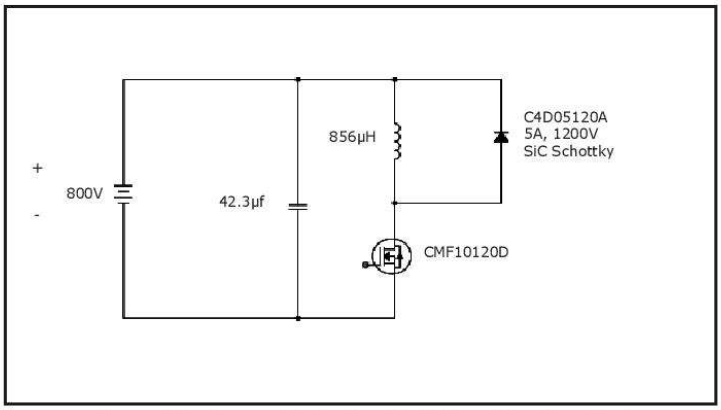


Figure 20. Clamped Inductive Switching Waveform Test Circuit

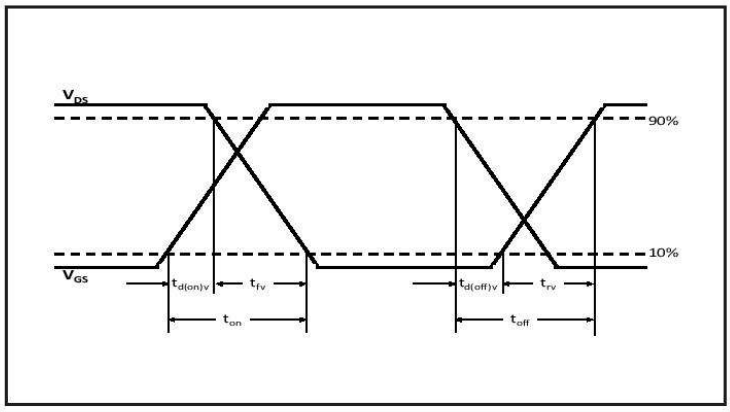


Figure 21. Switching Test Waveforms for Transition times

Test Circuit Diagrams and Waveforms

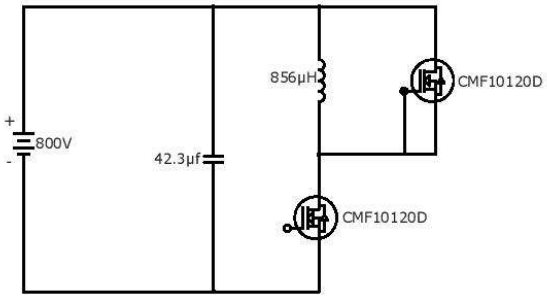


Fig 22. Body Diode Recovery Test

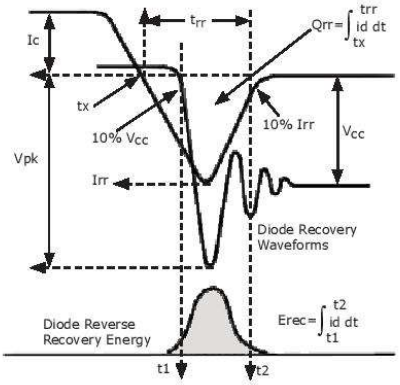


Fig 23. Body Diode Recovery Waveform

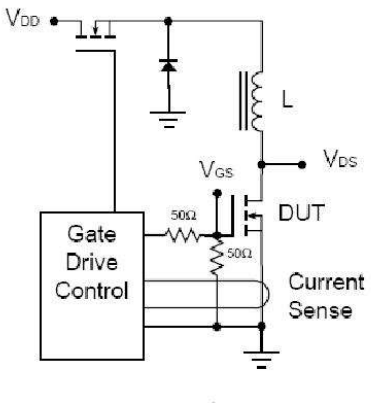
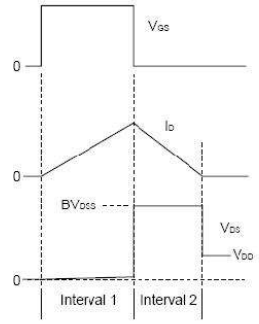


Fig 24. Unclamped Inductive Switching Test Circuit



$$E_A = 1/2L \times I_D^2$$

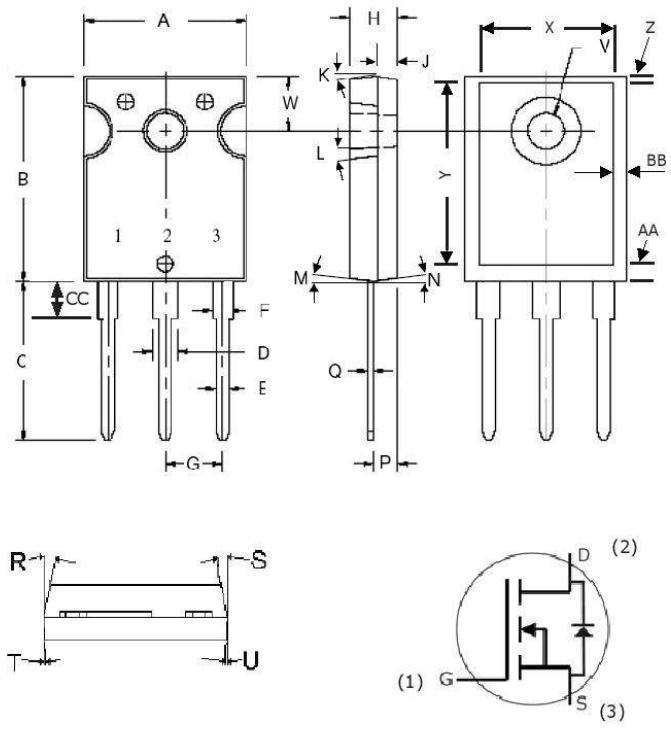
Fig 25. Unclamped Inductive Switching waveform for Avalanche Energy

ESD Ratings

ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

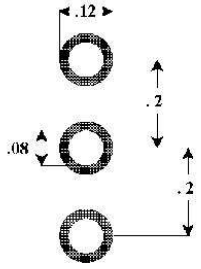
Package Dimensions

Package TO-247-3



POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.605	.635	15.367	16.130
B	.800	.831	20.320	21.10
C	.780	.800	19.810	20.320
D	.095	.133	2.413	3.380
E	.046	.052	1.168	1.321
F	.060	.095	1.524	2.410
G	.215 TYP		5.460 TYP	
H	.175	.205	4.450	5.210
J	.075	.085	1.910	2.160
K	6°	21°	6°	21°
L	4°	6°	4°	6°
M	2°	4°	2°	4°
N	2°	4°	2°	4°
P	.090	.100	2.286	2.540
Q	.020	.030	.508	.762
R	9°	11°	9°	11°
S	9°	11°	9°	11°
T	2°	8°	2°	8°
U	2°	8°	2°	8°
V	.137	.144	3.487	3.658
W	.210	.248	5.334	6.300
X	.502	.557	12.751	14.150
Y	.637	.695	16.180	17.653
Z	.038	.052	0.964	1.321
AA	.110	.140	2.794	3.556
BB	.030	.046	0.766	1.168
CC	.161	.176	4.100	4.472

Recommended Solder Pad Layout



TO-247-3

Part Number	Package	Marking
CMF10120D	TO-247-3	CMF10120

"The levels of environmentally sensitive, persistent biologically toxic (PBT), persistent organic pollutants (POP), or otherwise restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), as amended through April 21, 2006.

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Fax: +1.919.313.5451
www.cree.com/power

CMF20120D-Silicon Carbide Power MOSFET

Z-FET™ MOSFET

N-Channel Enhancement Mode

V_{DS}	1200 V
$I_{D(MAX)}$	42 A
$R_{DS(on)}$	80mΩ

Features

- High Speed Switching with Low Capacitances
- High Blocking Voltage with Low $R_{DS(on)}$
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased System Switching Frequency

Applications

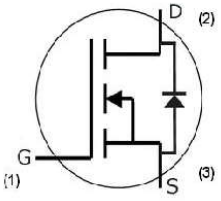
- Solar Inverters
- High Voltage DC/DC Converters
- Motor Drives
- Switch Mode Power Supplies
- UPS

Package

TO-247-3

Halogen-Free

RoHS COMPLIANT



Part Number	Package
CMF20120D	TO-247-3

Maximum Ratings (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
I_D	Continuous Drain Current	42	A	V_{GS}@20V, T_C = 25°C	Fig. 10
		24		V_{GS}@20V, T_C = 100°C	
I_{Dpulse}	Pulsed Drain Current	90	A	Pulse width t_P limited by T_{jmax} T_C = 25°C	
E_{AS}	Single Pulse Avalanche Energy	2.2	J	I_D = 20A, V_{DD} = 50 V, L = 9.5 mH	Fig. 15
E_{AR}	Repetitive Avalanche Energy	1.5	J	t_{AR} limited by T_{jmax}	
I_{AR}	Repetitive Avalanche Current	20	A	I_D = 20A, V_{DD} = 50 V, L = 3 mH t_{AR} limited by T_{jmax}	
V_{GS}	Gate Source Voltage	-5/+25	V		
P_{tot}	Power Dissipation	215	W	T_C=25°C	Fig. 9
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +135	°C		
T_L	Solder Temperature	260	°C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0V, I_D = 100µA	
$V_{GS(th)}$	Gate Threshold Voltage		2.65	4	V	V_{DS} = V_{GS}, I_D = 1mA	Fig. 11
			3.2	4.8		V_{DS} = V_{GS}, I_D = 10mA	
			2.0		V	V_{DS} = V_{GS}, I_D = 1mA, T_J = 135ºC	
			2.45			V_{DS} = V_{GS}, I_D = 10mA, T_J = 135ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	µA	V_{DS} = 1200V, V_{GS} = 0V	
			10	250		V_{DS} = 1200V, V_{GS} = 0V, T_J = 135ºC	
I_{GSS}	Gate-Source Leakage Current			0.25	µA	V_{GS} = 20V, V_{DS} = 0V	
$R_{DS(on)}$	Drain-Source On-State Resistance		80	100	mΩ	V_{GS} = 20V, I_D = 20A	Fig. 3
			95	120		V_{GS} = 20V, I_D = 20A, T_J = 135ºC	
g_{fs}	Transconductance		7.9		S	V_{DS}= 20V, I_{DS}= 20A	Fig. 6
			7.4			V_{DS}= 20V, I_{DS}= 20A, T_J = 135ºC	
C_{iss}	Input Capacitance		1915		pF	V_{GS} = 0V V_{DS} = 800V f = 1MHz V_{AC} = 25mV	Fig. 13
C_{oss}	Output Capacitance		120				
C_{rss}	Reverse Transfer Capacitance		13				
E_{oss}	C_{oss} Stored Energy		62		µJ		Fig. 14
$t_{d(on)v}$	Turn-On Delay Time		13		ns	V_{DD} = 800V, V_{GS} = 0/20V I_D = 20A $R_{G(ext)}$ = 2.5Ω, R_L = 40Ω Timing relative to V_{DS}	Fig. 17
t_{fv}	Fall Time		24				
$t_{d(off)v}$	Turn-Off Delay Time		40				
t_{rv}	Rise Time		38				
R_G	Internal Gate Resistance		5		Ω	f = 1MHz, V_{AC} = 25mV	

Built-in SiC Body Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.5		V	V_{GS} = -5V, I_F=10A, T_J = 25ºC	
		3.1			V_{GS} = -2V, I_F=10A, T_J = 25ºC	
t_{rr}	Reverse Recovery Time	220		ns	V_{GS} = -5V, I_F=20A, T_J = 25ºC V_R = 800V, di_F/dt= 100A/µs	Fig. 22
Q_{rr}	Reverse Recovery Charge	142		nC		
I_{rrm}	Peak Reverse Recovery Current	2.3		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.44	0.51	K/W		Fig. 7
$R_{\theta CS}$	Case to Sink, w/ Thermal Compound	0.25				
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient		40			

Gate Charge Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
Q_{gs}	Gate to Source Charge	23.8		nC	V_{DD} = 800V, V_{GS} = 0/20V I_D =20A Per JEDEC24 pg 27	Fig. 12
Q_{gd}	Gate to Drain Charge	43.1				
Q_g	Gate Charge Total	90.8				

Typical Performance

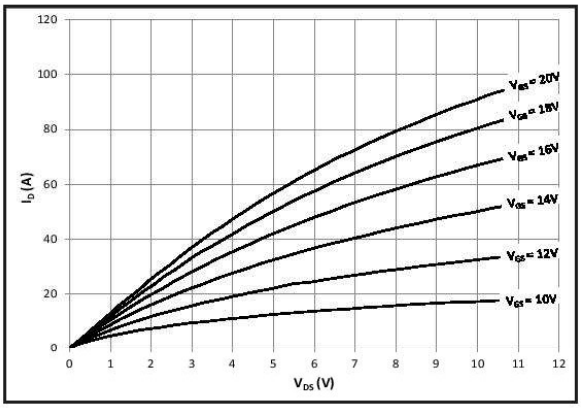


Figure 1. Typical Output Characteristics T_J = 25ºC

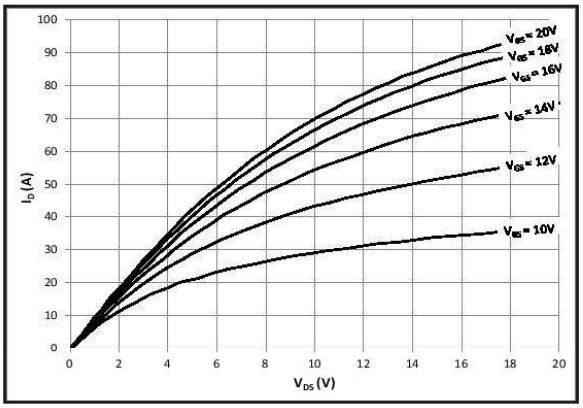


Figure 2. Typical Output Characteristics T_J = 135ºC

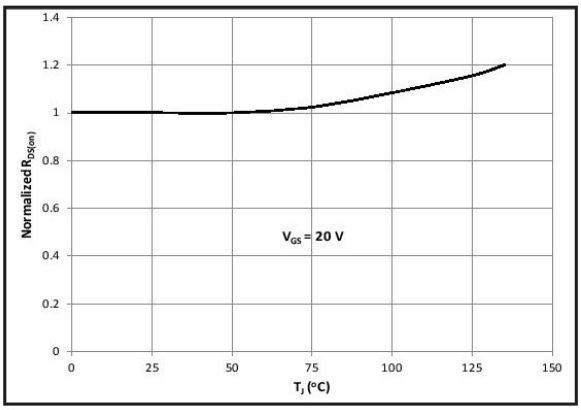


Figure 3. Normalized On-Resistance vs. Temperature

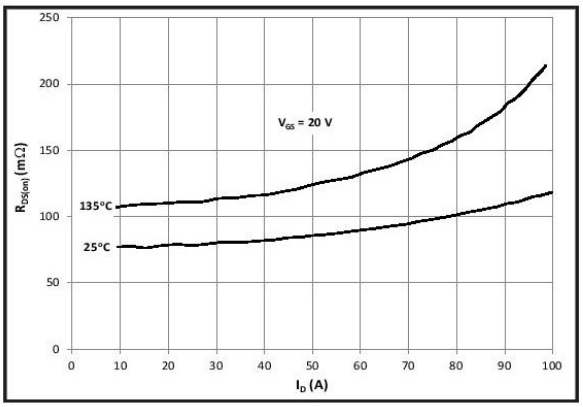


Figure 4. On-Resistance vs. Drain Current

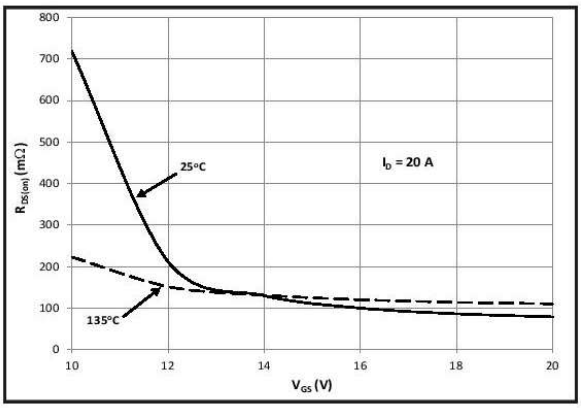


Figure 5. On-Resistance vs. Gate Voltage

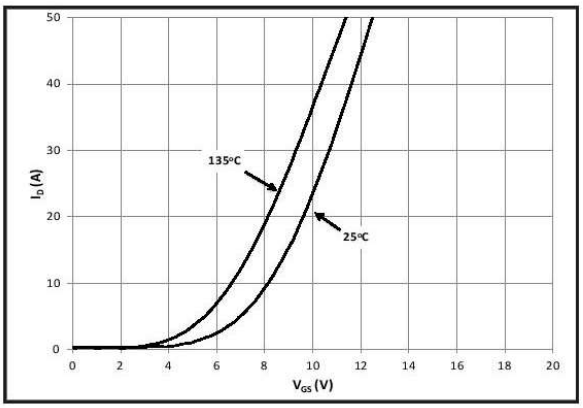


Figure 6. Typical Transfer Characteristics

Typical Performance

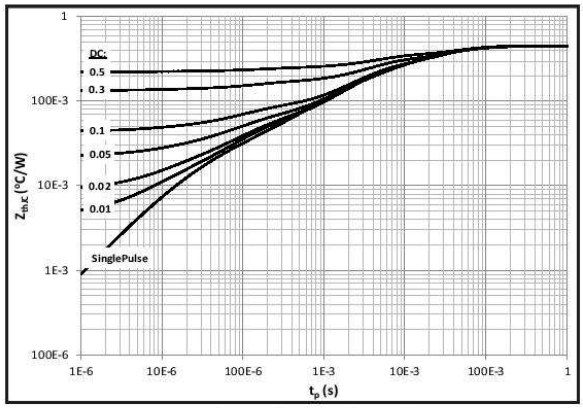


Figure 7. Transient Thermal Impedance (Junction - Case) with Duty Cycle

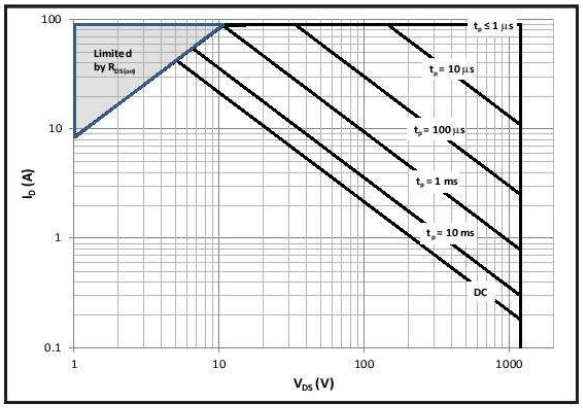


Figure 8. Safe Operating Area

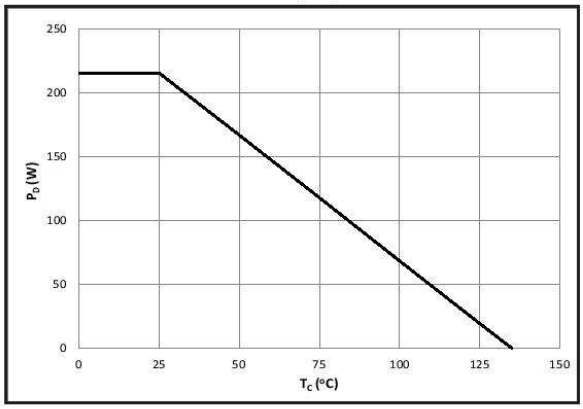


Figure 9. Power Dissipation Derating Curve

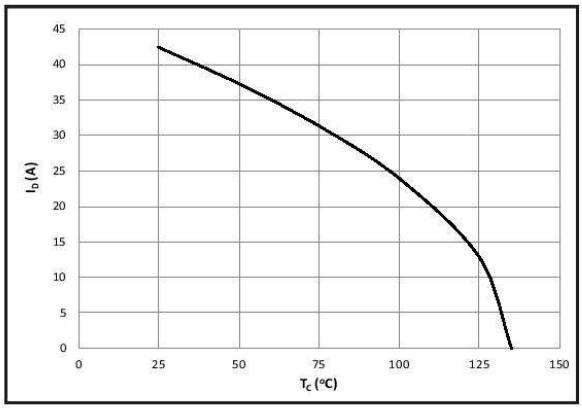


Figure 10. Continuous Current Derating Curve

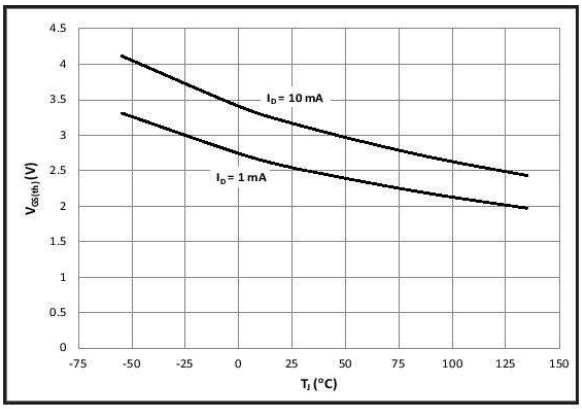


Figure 11. Gate Threshold Voltage vs. Temperature

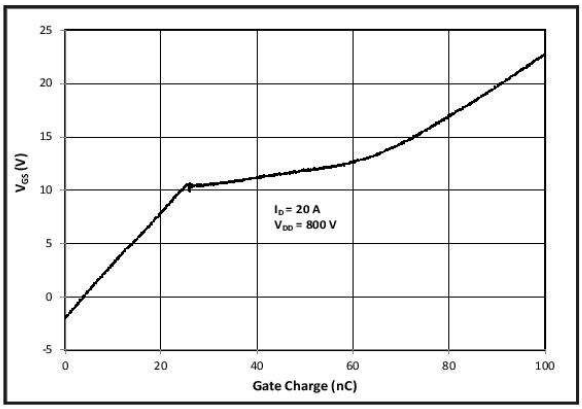
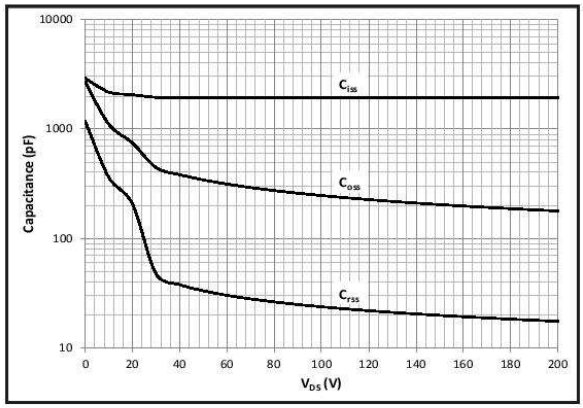


Figure 12. Typical Gate Charge Characteristics (25°C)

Typical Performance



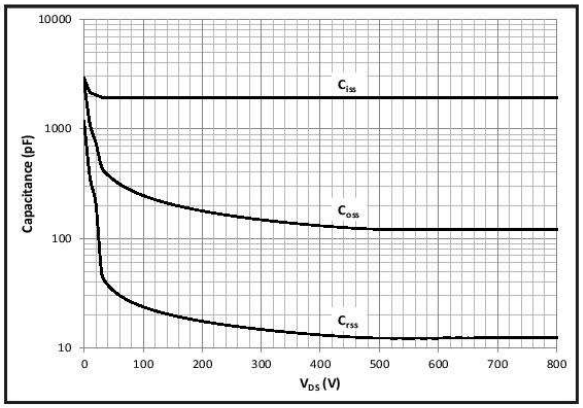


Figure 13A and 13B. Typical Capacitances vs. Drain Voltage at V_{GS} = 0V and f = 1 MHz

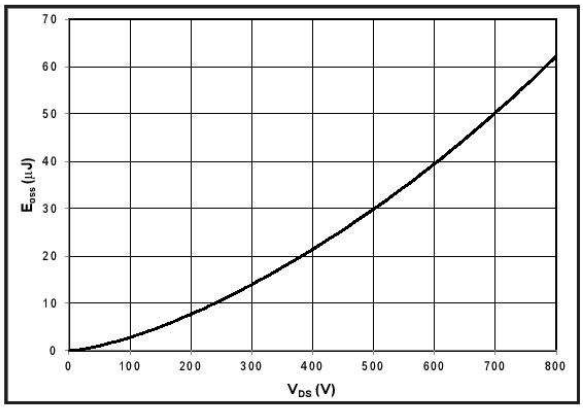


Figure 14. Typical C_{OSS} Stored Energy

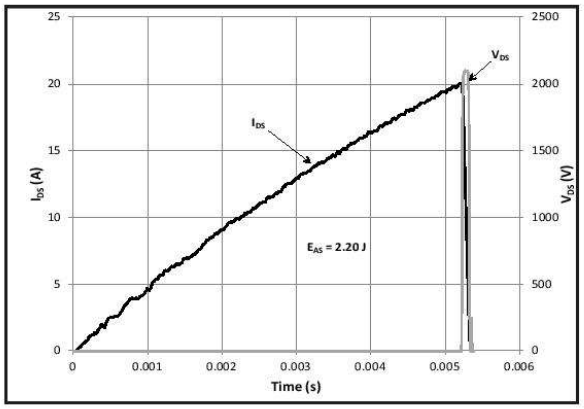


Figure 15. Typical Unclamped Inductive Switching Waveforms Showing Avalanche Capability

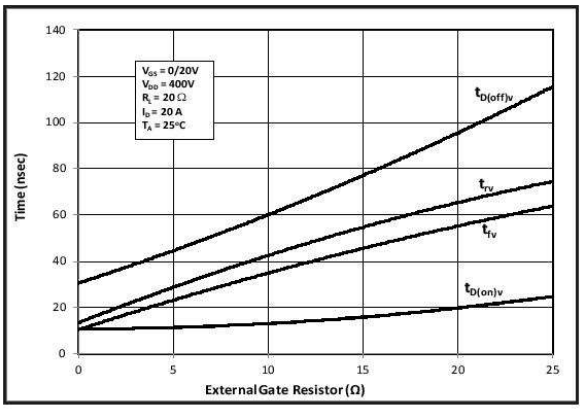


Figure 16. Resistive Switching Times vs. External R_G at V_{DD} = 400V, I_D = 20A

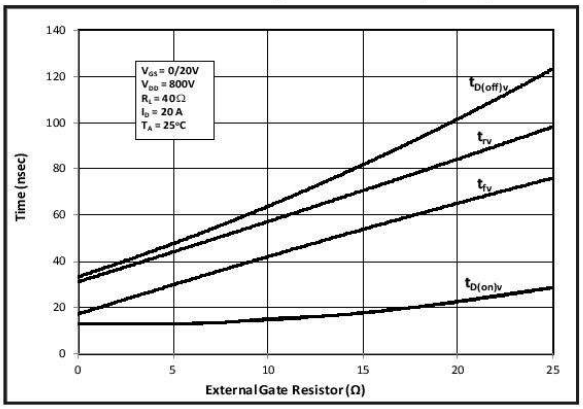


Figure 17. Resistive Switching Times vs. External R_G at V_{DD} = 800V, I_D = 20A

Typical Performance

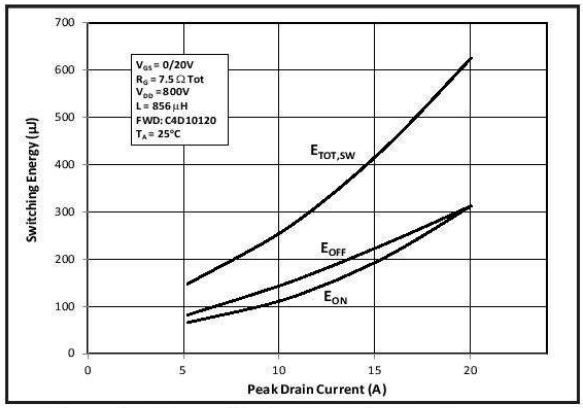


Figure 18. Clamped Inductive Switching Energy vs. Drain Current (Fig. 20)

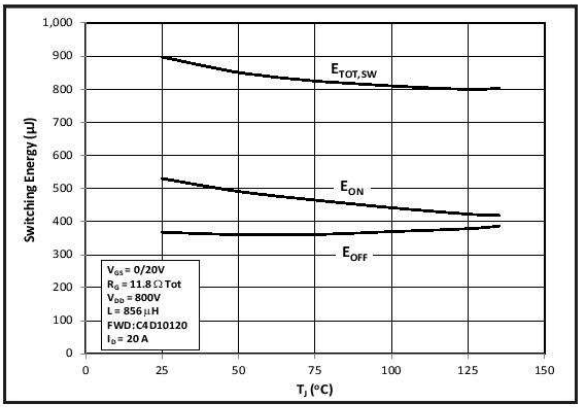


Figure 19. Clamped Inductive Switching Energy vs. Junction Temperature (Fig 20)

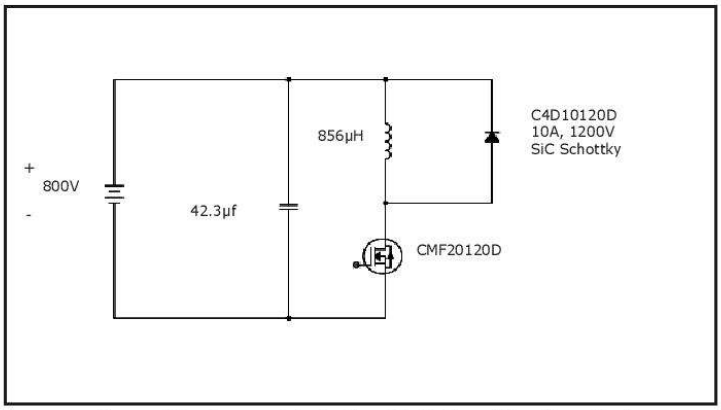


Figure 20. Clamped Inductive Switching Waveform Test Circuit

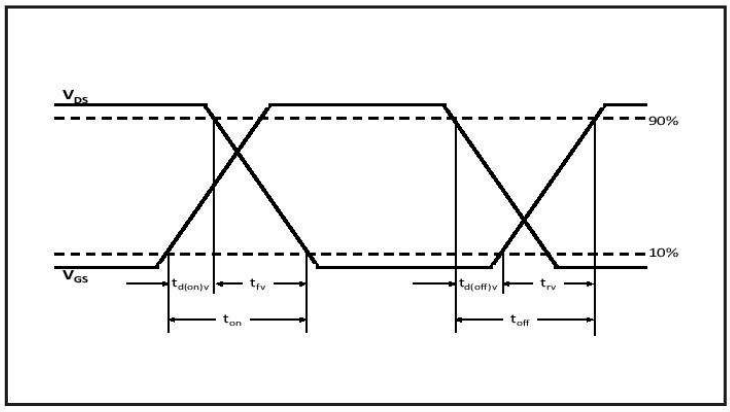


Figure 21. Switching Test Waveforms for Transition times

Test Circuit Diagrams and Waveforms

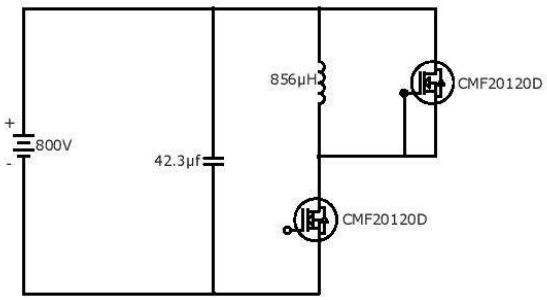


Fig 22. Body Diode Recovery Test

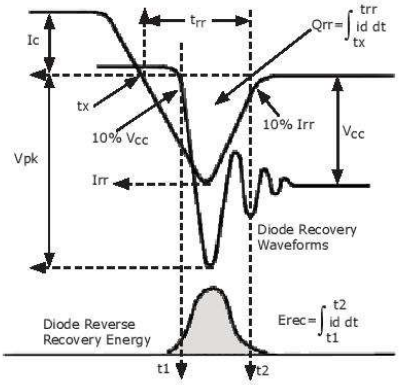


Fig 23. Body Diode Recovery Waveform

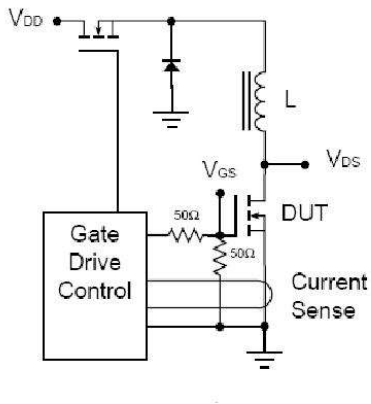
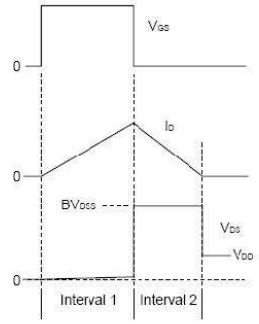


Fig 24. Unclamped Inductive Switching Test Circuit



$$E_A = 1/2L \times I_D^2$$

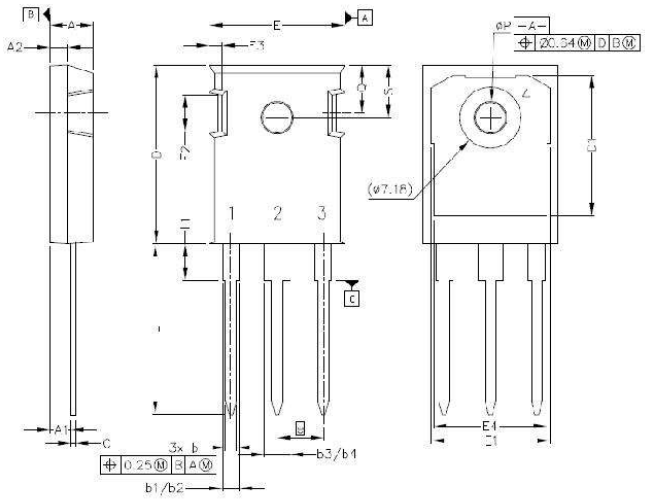
Fig 25. Unclamped Inductive Switching waveform for Avalanche Energy

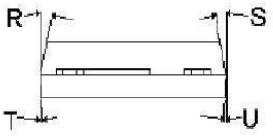
ESD Ratings

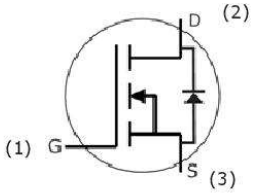
ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

Package Dimensions

Package TO-247-3

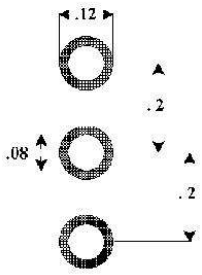






POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30

Recommended Solder Pad Layout



TO-247-3

Part Number	Package	Marking
CMF20120D	TO-247-3	CMF20120

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power

FAIRCHILD SEMICONDUCTOR®

May 2006

FGA15N120ANTD
1200V NPT Trench IGBT

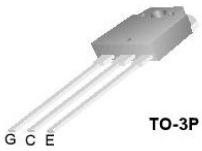
Features

- NPT Trench Technology, Positive temperature coefficient
- Low saturation voltage: $V_{CE(sat),\ typ}$ = 1.9V @ I_C = 15A and T_C = 25°C
- Low switching loss: $E_{off,\ typ}$ = 0.6mJ @ I_C = 15A and T_C = 25°C
- Extremely enhanced avalanche capability

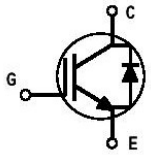
Description

Using Fairchild's proprietary trench design and advanced NPT technology, the 1200V NPT IGBT offers superior conduction and switching performances, high avalanche ruggedness and easy parallel operation.

This device is well suited for the resonant or soft switching application such as induction heating, microwave oven, etc.



TO-3P



Absolute Maximum Ratings

Symbol	Description		FGA15N120ANTD	Units
V_{CES}	Collector-Emitter Voltage		1200	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Current	@ T_C = 25°C	30	A
	Collector Current	@ T_C = 100°C	15	A
I_{CM}	Pulsed Collector Current (Note 1)		45	A
I_F	Diode Continuous Forward Current	@ T_C = 100°C	15	A
I_{FM}	Diode Maximum Forward Current		45	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	186	W
	Maximum Power Dissipation	@ T_C = 100°C	74	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for IGBT	–	0.67	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for Diode	–	2.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	–	40	°C/W

Notes:
(1) Repetitive rating: Pulse width limited by max. junction temperature

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FGA15N120ANTD	FGA15N120ANTD	TO-3P	–	--	30

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
I_{CES}	Collector Cut-Off Current	V_{CE} = V_{CES}, V_{GE} = 0V	–	–	3	mA
I_{GES}	G-E Leakage Current	V_{GE} = V_{GES}, V_{CE} = 0V	–	–	± 250	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 15mA, V_{CE} = V_{GE}	4.5	6.5	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 15A. V_{GE} = 15V	–	1.9	2.4	V
		I_C = 15A. V_{GE} = 15V, T_C = 125°C	–	2.2	--	V
		I_C = 30A, V_{GE} = 15V	–	2.3	--	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30V, V_{GE} = 0V, f = 1MHz	–	2650	--	pF
C_{oes}	Output Capacitance		–	143	--	pF
C_{res}	Reverse Transfer Capacitance		–	96	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15A, R_G = 10Ω, V_{GE} = 15V, Inductive Load, T_C = 25°C	–	15	--	ns
t_r	Rise Time		–	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		–	160	--	ns
t_f	Fall Time		–	100	180	ns
E_{on}	Turn-On Switching Loss		–	3	4.5	mJ
E_{off}	Turn-Off Switching Loss		–	0.6	0.9	mJ
E_{ts}	Total Switching Loss		–	3.6	5.4	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15A, R_G = 10Ω, V_{GE} = 15V, Inductive Load, T_C = 125°C	–	15	--	ns
t_r	Rise Time		–	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		–	170	--	ns
t_f	Fall Time		–	150	--	ns
E_{on}	Turn-On Switching Loss		–	3.2	4.8	mJ
E_{off}	Turn-Off Switching Loss		–	0.8	1.2	mJ
E_{ts}	Total Switching Loss		–	4.0	6.0	mJ
Q_g	Total Gate Charge	V_{CE} = 600 V, I_C = 15A, V_{GE} = 15V	–	120	180	nC
Q_{ge}	Gate-Emitter Charge		–	16	22	nC
Q_{gc}	Gate-Collector Charge		–	50	65	nC

Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
V_{FM}	Diode Forward Voltage	I_F = 15A	T_C = 25°C	--	1.7	2.7	V
			T_C = 125°C	--	1.8	--	
t_{rr}	Diode Reverse Recovery Time	I_F = 15A dI/dt = 200 A/μs	T_C = 25°C	--	210	330	ns
			T_C = 125°C	--	280	--	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	--	27	40	A
			T_C = 125°C	--	31	--	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	--	2835	6600	nC
			T_C = 125°C	--	4340	--	

Typical Performance Characteristics

Figure 1. Typical Output Characteristics

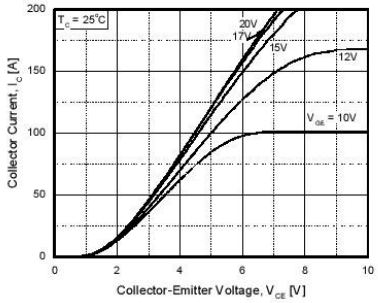


Figure 2. Typical Saturation Voltage Characteristics

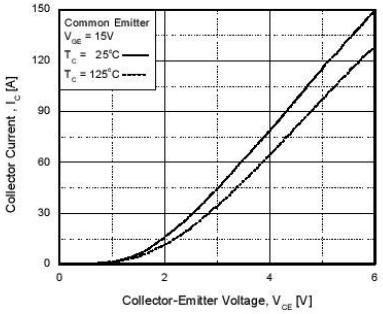


Figure 3. Saturation Voltage vs. Case Temperature at Variant Current Level

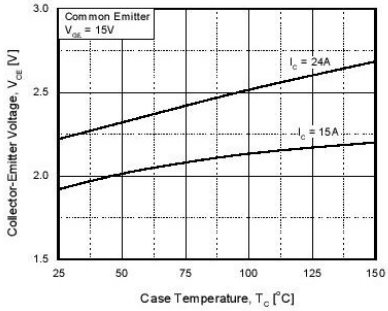


Figure 4. Saturation Voltage vs. V_{GE}

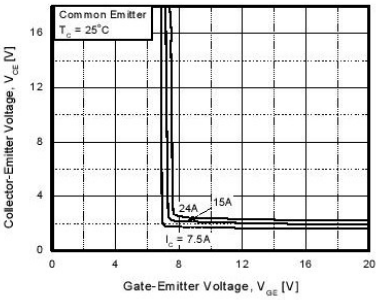


Figure 5. Saturation Voltage vs. V_{GE}

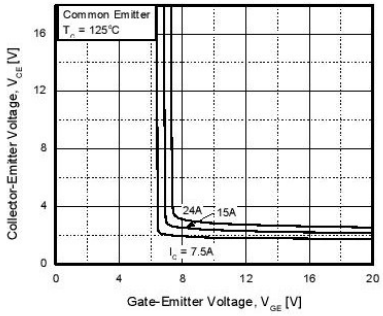
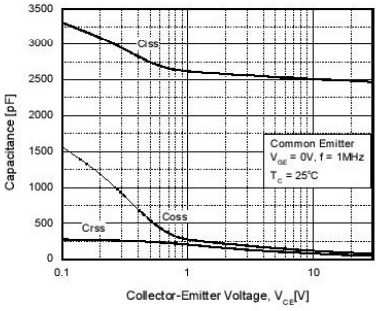


Figure 6. Capacitance Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Turn-On Characteristics vs. Gate Resistance

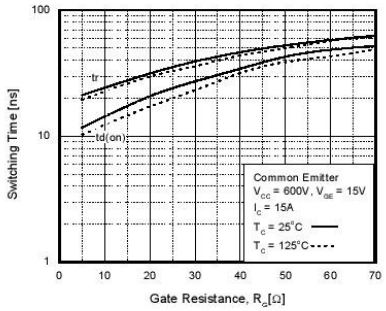


Figure 8. Turn-Off Characteristics vs. Gate Resistance

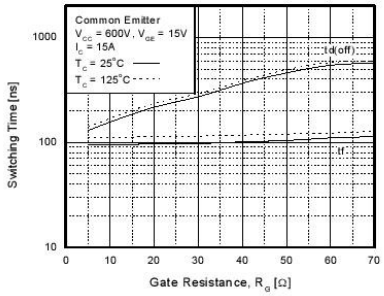


Figure 9. Switching Loss vs. Gate Resistance

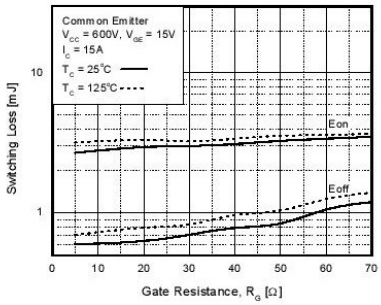


Figure 10. Turn-On Characteristics vs. Collector Current

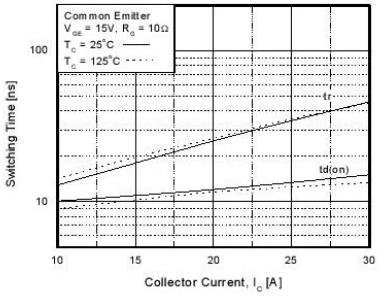


Figure 11. Turn-Off Characteristics vs. Collector Current

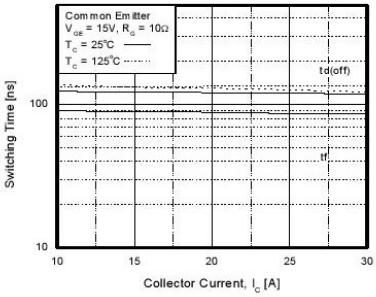
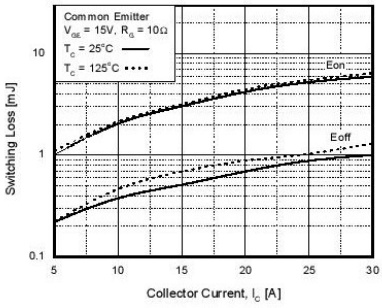


Figure 12. Switching Loss vs. Collector Current



Typical Performance Characteristics (Continued)

Figure 13. Gate Charge Characteristics

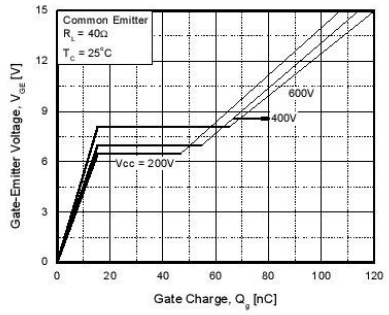


Figure 14. SOA Characteristics

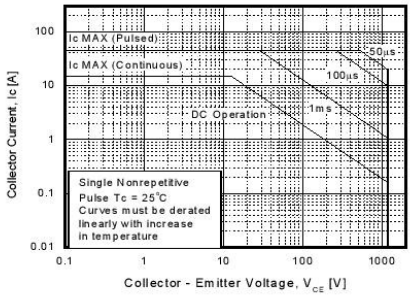


Figure 15. Turn-Off SOA

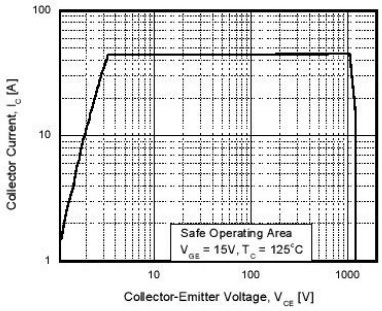
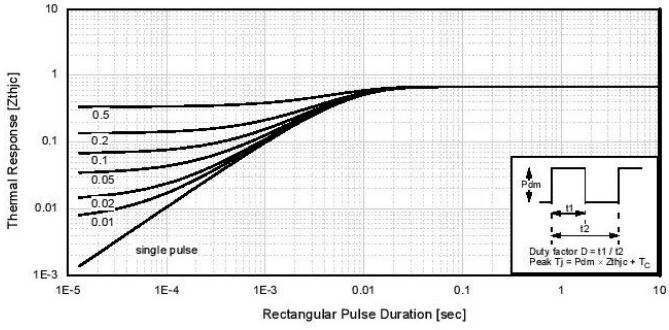


Figure 16. Transient Thermal Impedance of IGBT



Typical Performance Characteristics (Continued)

Figure 17. Forward Characteristics

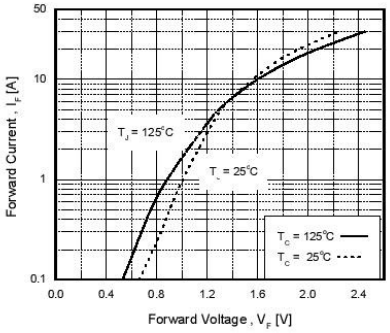


Figure 18. Reverse Recovery Current

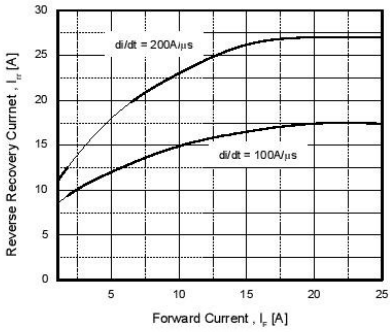


Figure 19. Stored Charge

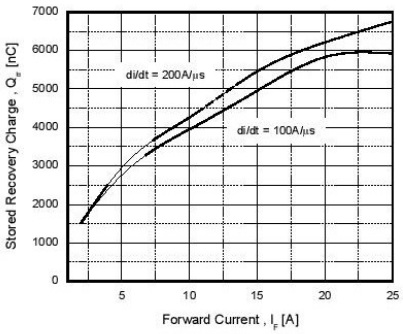
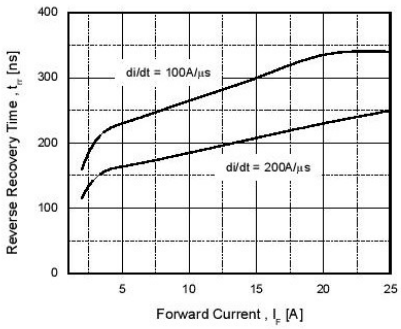
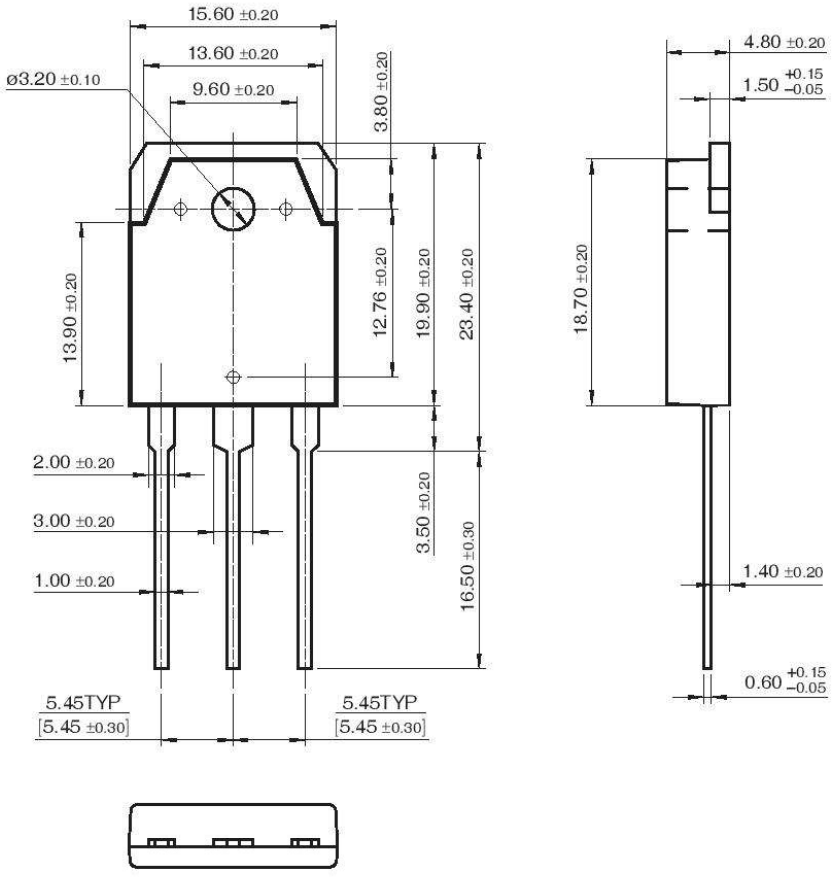


Figure 20. Reverse Recovery Time



Mechanical Dimensions

TO-3P



Dimensions in Millimeters

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Bottomless™	FPS™	MICROCOUPLER™	PowerTrench®	SuperSOT™-6
Build it Now™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CoolFET™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
CROSSVOLT™	GTO™	MICROWIRE™	QT Optoelectronics™	TCM™
DOME™	HiSeC™	MSX™	Quiet Series™	TinyLogic®
EcoSPARK™	I^2C™	MSXPro™	RapidConfigure™	TINYOPTO™
E^2CMOS™	*i-Lo*™	OCX™	RapidConnect™	TruTranslation™
EnSigna™	ImpliedDisconnect™	OCXPro™	µSerDes™	UHC™
FACT™	IntelliMAX™	OPTOLOGIC®	ScalarPump™	UniFET™
FACT Quiet Series™		OPTOPLANAR™	SILENT SWITCHER®	UltraFET®
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The Power Franchise®		POP™	SPM™	Wire™
Programmable Active Droop™		Power247™	Stealth™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I19

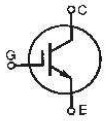
IXYS

GenX3™ 1200V IGBTs

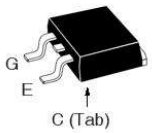
IXGA20N120A3
IXGP20N120A3
IXGH20N120A3

V_{CES} = 1200V
I_{C110} = 20A
$V_{CE(sat)}$ ≤ 2.5V

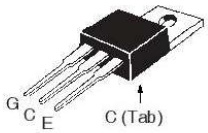
Ultra-Low Vsat PT IGBTs for
up to 3 kHz Switching



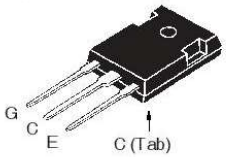
TO-263 AA (IXGA)



TO-220AB (IXGP)



TO-247 (IXGH)



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1200	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1200	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	40	A
I_{C110}	T_C = 110°C	20	A
I_{CM}	T_C = 25°C, 1ms	120	A
SSOA	V_{GE} = 15V, T_J = 125°C, R_G = 10Ω	I_{CM} = 40	A
(RBSOA)	Clamped Inductive Load	@V_{CE} ≤ 960	V
P_C	T_C = 25°C	180	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting Torque (TO-247 & TO-220)	1.13/10	Nm/lb.in.
F_C	Mounting Force (TO-263)	10..65 / 2.2..14.6	N/lb.
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6mm (0.062 in.) from Case for 10s	260	°C
Weight	TO-263	2.5	g
	TO-220	3.0	g
	TO-247	6.0	g

Symbol	Test Conditions	Characteristic Values			
(T_J = 25°C, Unless Otherwise Specified)		Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	1200			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	2.5		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			25	μA
	T_J = 125°C			1	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 20A, V_{GE} = 15V, Note 1		2.3	2.5	V
	T_J = 125°C		2.5		V

Features

- Optimized for Low Conduction Losses
- International Standard Packages

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

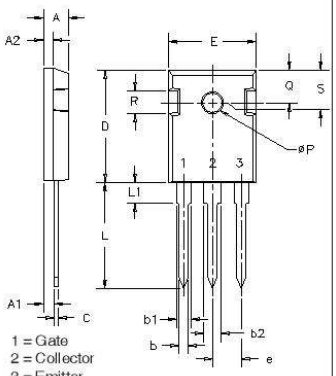
- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- Inrush Current Protection Circuits

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 20A, V_{CE} = 10V, Note 1	7	12	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		1075	pF
C_{oes}			80	pF
C_{res}			27	pF
Q_g	I_C = 20A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		50	nC
Q_{ge}			7.3	nC
Q_{gc}			23	nC
$t_{d(on)}$	**Inductive Load, T_J = 25°C**		16	ns
t_{ri}	I_C = 20A, V_{GE} = 15V		44	ns
E_{on}	V_{CE} = 960V, R_G = 10Ω		2.85	mJ
$t_{d(off)}$	Note 2		290	ns
t_{fi}			715	ns
E_{off}			6.47	mJ
$t_{d(on)}$	**Inductive Load, T_J = 125°C**		16	ns
t_{ri}	I_C = 20A, V_{GE} = 15V		50	ns
E_{on}	V_{CE} = 960V, R_G = 10Ω		5.53	mJ
$t_{d(off)}$	Note 2		310	ns
t_{fi}			1220	ns
E_{off}			10.10	mJ
R_{thJC}				0.69 °C/W
R_{thCK}	TO-220		0.50	°C/W
	TO-247		0.21	°C/W

Notes:

1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.
2. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

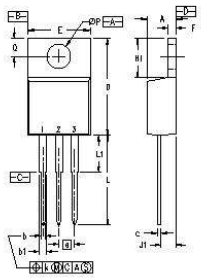
TO-247 (IXGH) AD Outline



1 = Gate
2 = Collector
3 = Emitter
Tab = Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.7	5.3
A_1	.087	.102	2.2	2.54
A_2	.059	.098	2.2	2.6
b	.040	.055	1.0	1.4
b_1	.065	.084	1.65	2.13
b_2	.113	.123	2.87	3.12
C	.016	.031	.4	.8
D	.819	.845	20.80	21.46
E	.610	.640	15.75	16.26
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1		.177		4.50
øP	.140	.144	3.55	3.65
Q	.212	.244	5.4	6.2
R	.170	.216	4.32	5.49
S	.242 BSC		6.15 BSC	

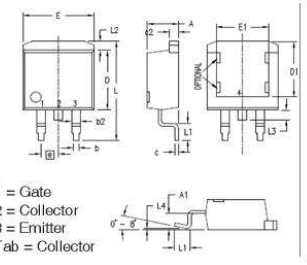
TO-220 (IXGP) Outline



Pins: 1 - Gate 2 - Collector
3 - Emitter 4 - Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
øP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

TO-263 (IXGA) Outline



1 = Gate
2 = Collector
3 = Emitter
Tab = Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

Fig. 1. Output Characteristics @ T_J = 25ºC

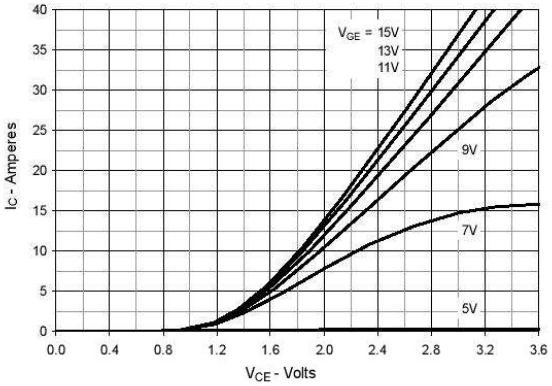


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

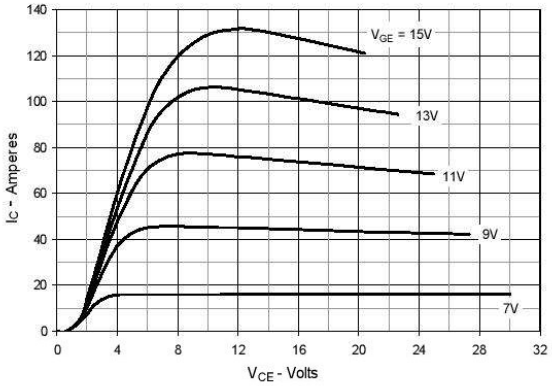


Fig. 3. Output Characteristics @ T_J = 125ºC

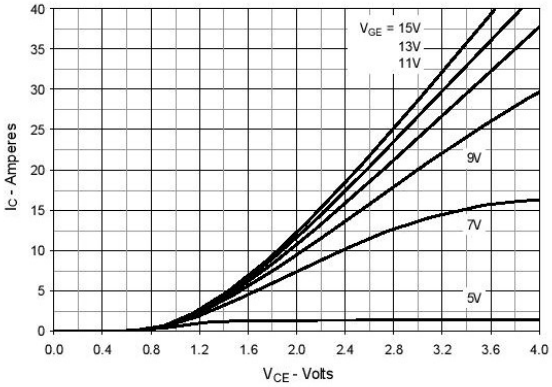


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

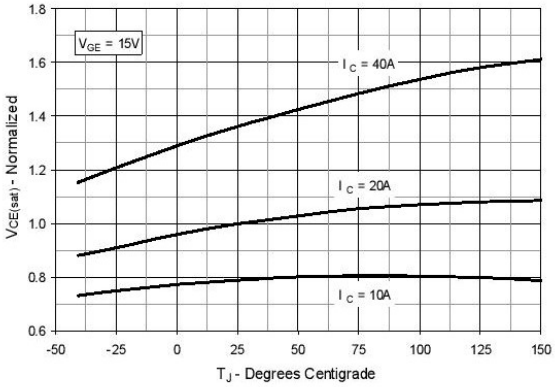


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

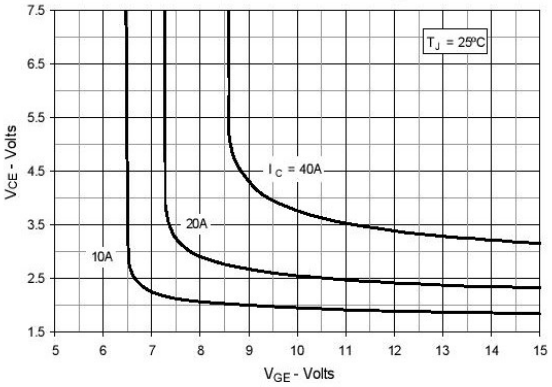


Fig. 6. Input Admittance

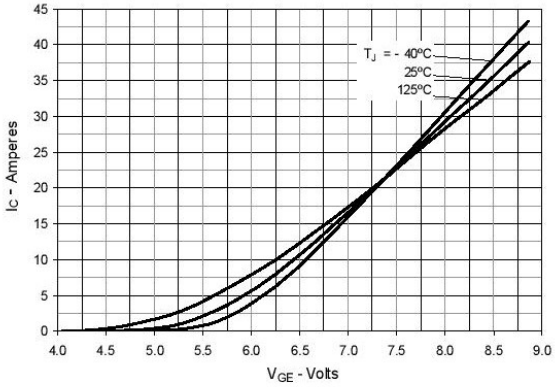


Fig. 7. Transconductance

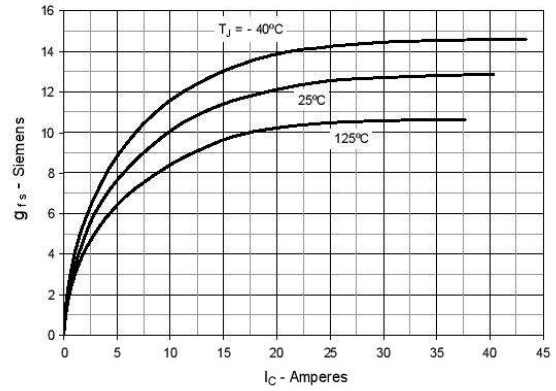


Fig. 8. Gate Charge

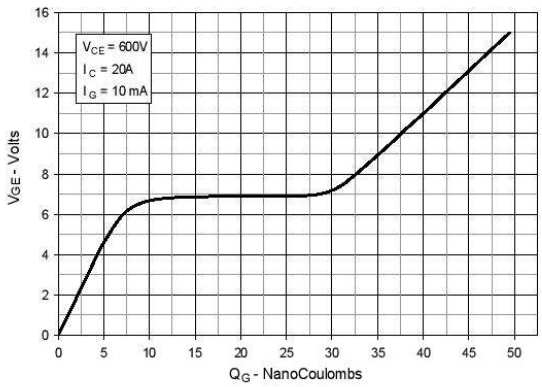


Fig. 9. Capacitance

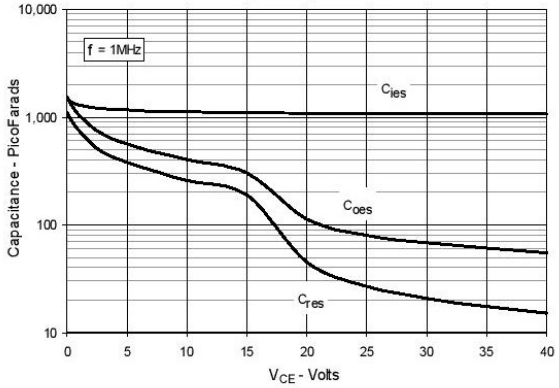


Fig. 10. Reverse-Bias Safe Operating Area

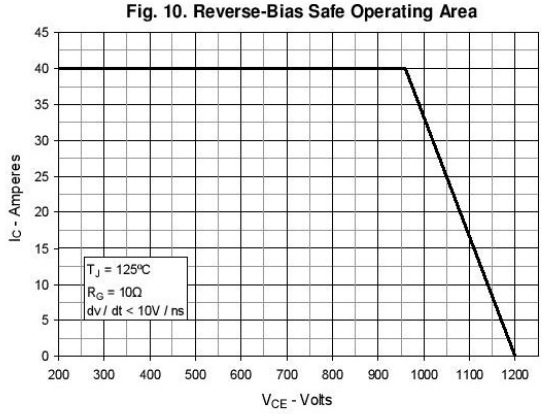


Fig. 11. Maximum Transient Thermal Impedance

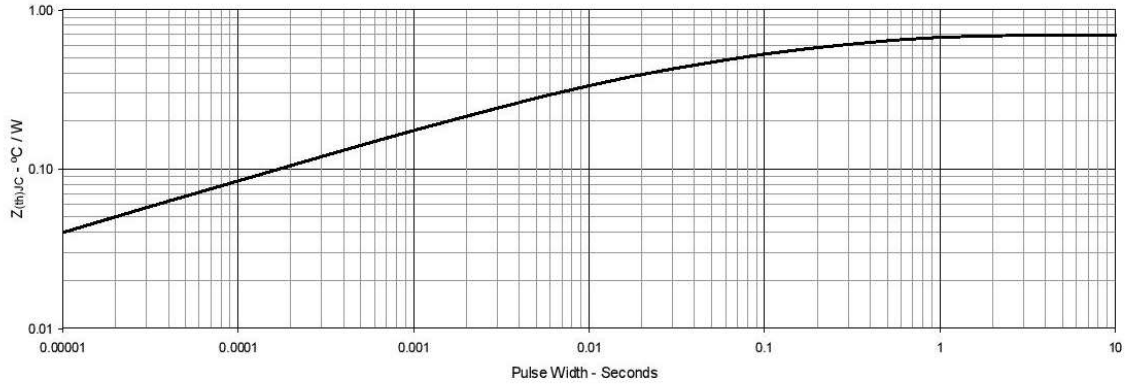


Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

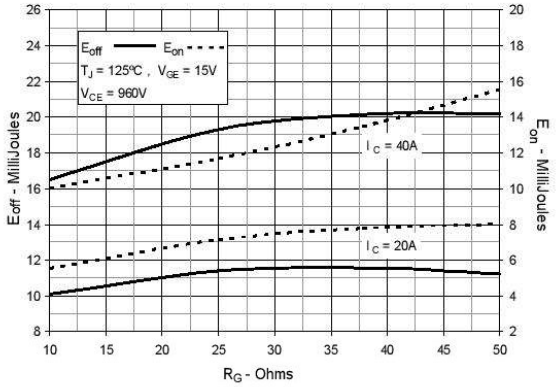


Fig. 13. Inductive Switching Energy Loss vs. Collector Current

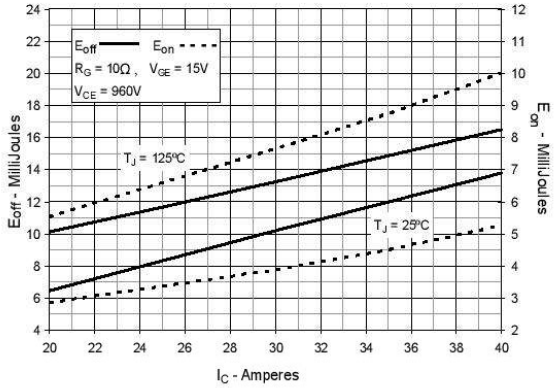


Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature

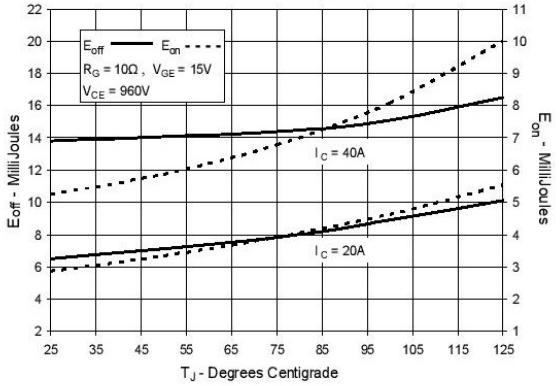


Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance

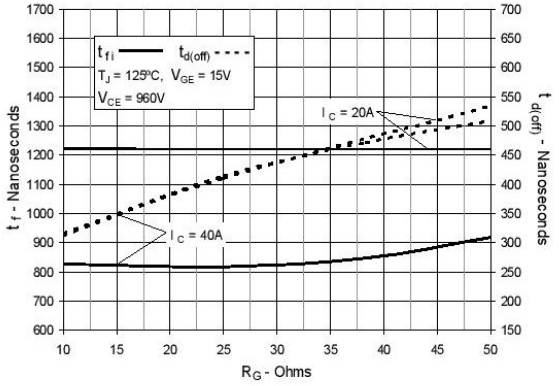


Fig. 16. Inductive Turn-off Switching Times vs. Collector Current

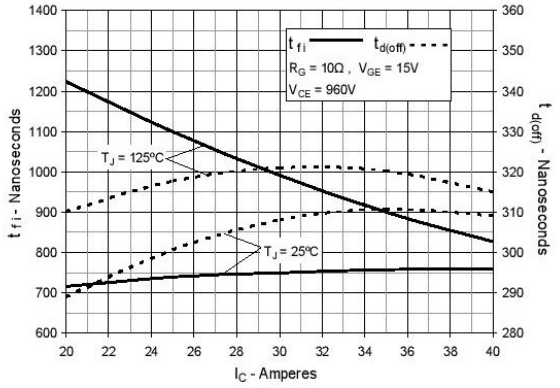


Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature

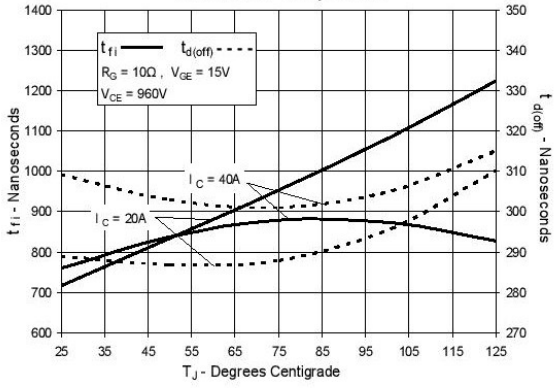


Fig. 18. Inductive Turn-on Switching Times vs. Gate Resistance

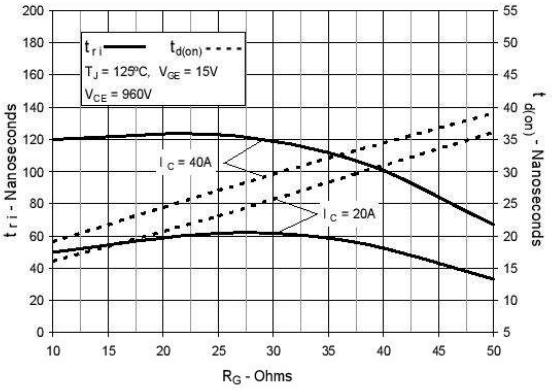


Fig. 19. Inductive Turn-on Switching Times vs. Collector Current

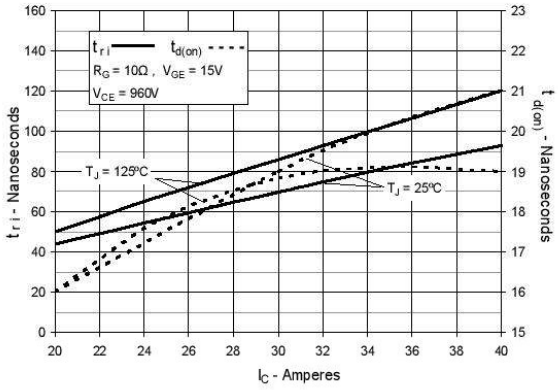


Fig. 20. Inductive Turn-on Switching Times vs. Junction Temperature